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# MS-7A95

ATX

Ver: 1.0

## Basinfall Platform

### CPU:

*Skylake X/Kabylake X*

### System Chipset:

*Kaby Lake PCH-X*

### Onboard Chip:

*HD Audio Codec:ALC1220*

*LAN-Intel I219+I211*

*SIO:NTC6795D*

*Dual Flash ROM: SPI 64 MB X2*

### Main Memory:

*DDRIV (UP to 2677MHz) \* 8DIMM (4 Channel)*

### ACPI:

*MPS*

### PWM:

*VR13 -IR35201*

### Expansion Slots:

*PCI Express (X16) Slot \* 2*

*PCI Express (X8) Slot \* 1*

*PCI Express (X4) Slot \* 1*

*PCI Express (X1 ) Slot \* 2*

### Other:

*SATA3.0 \*8*

*USB2.0 \*6 Ports (2R/4F)*

*REAR USB30\*5 + USB3.1\*1 & TYPEC\*1*

*FRONT USB3.0 \*4+TYPEC\*1*

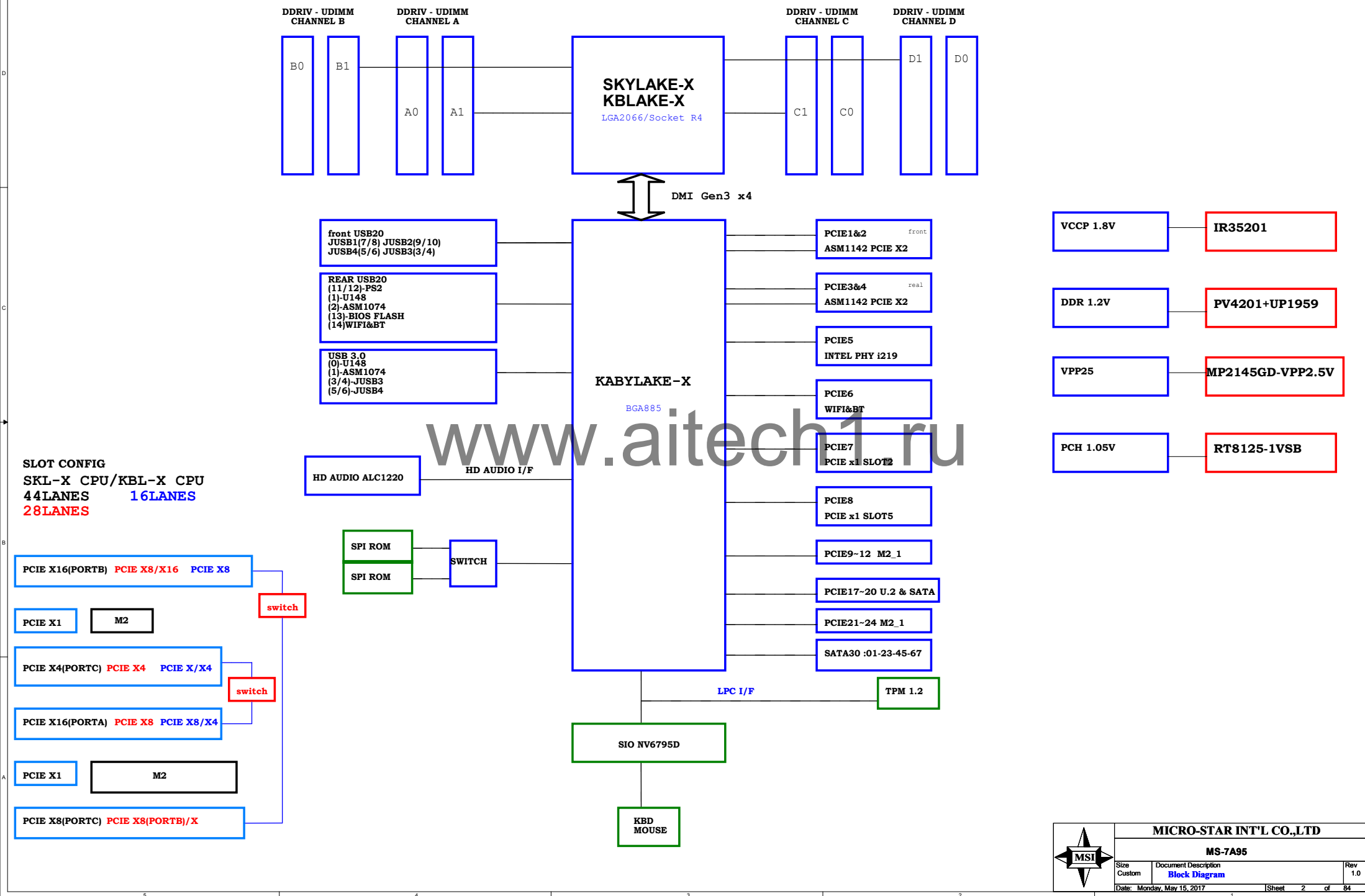


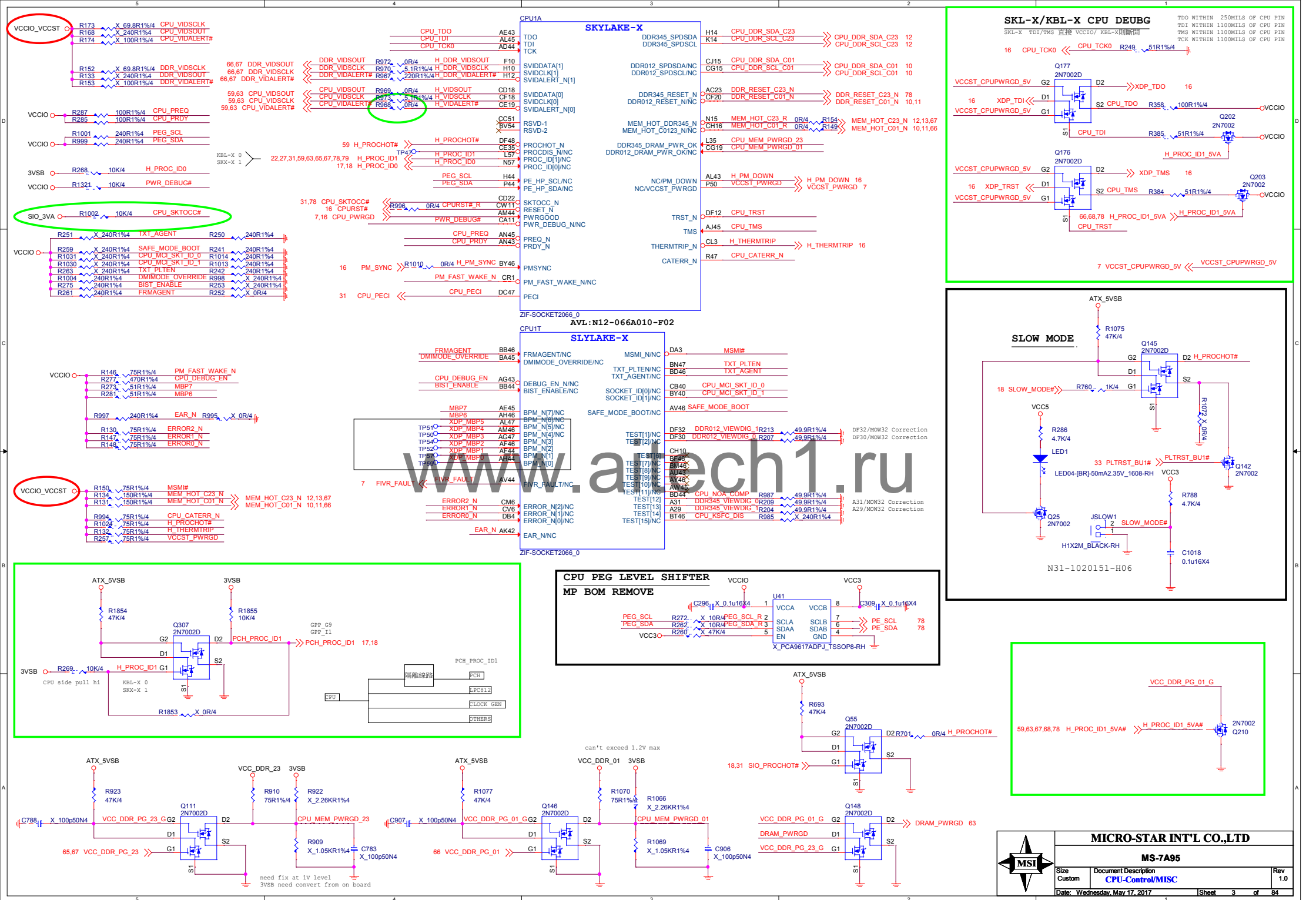
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Size Custom	Document Description <a href="#">Cover Sheet</a>	Rev 1.0
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## MS-7A95 Block Diagram





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CPU1B		
SKYLAKE-X		
MEM_MA_DATA63	DD52	DDR0_DQ[63]/NC
MEM_MA_DATA62	DD51	DDR0_DQ[62]/NC
MEM_MA_DATA61	DD48	DDR0_DQ[61]/NC
MEM_MA_DATA60	DD48	DDR0_DQ[60]/NC
MEM_MA_DATA59	DD48	DDR0_DQ[59]/NC
MEM_MA_DATA58	DD52	DDR0_DQ[58]/NC
MEM_MA_DATA57	DD48	DDR0_DQ[57]/NC
MEM_MA_DATA56	DE49	DDR0_DQ[56]/NC
MEM_MA_DATA55	CP48	DDR0_DQ[55]/NC
MEM_MA_DATA54	CV48	DDR0_DQ[54]/NC
MEM_MA_DATA53	CP48	DDR0_DQ[53]/NC
MEM_MA_DATA52	CP48	DDR0_DQ[52]/NC
MEM_MA_DATA51	CR49	DDR0_DQ[51]/NC
MEM_MA_DATA50	CU49	DDR0_DQ[50]/NC
MEM_MA_DATA49	CV48	DDR0_DQ[49]/NC
MEM_MA_DATA48	CR49	DDR0_DQ[48]/NC
MEM_MA_DATA47	DD46	DDR0_DQ[47]/NC
MEM_MA_DATA46	DE45	DDR0_DQ[46]/NC
MEM_MA_DATA45	DB42	DDR0_DQ[45]/NC
MEM_MA_DATA44	DD42	DDR0_DQ[44]/NC
MEM_MA_DATA43	DA45	DDR0_DQ[43]/NC
MEM_MA_DATA42	DB46	DDR0_DQ[42]/NC
MEM_MA_DATA41	DE43	DDR0_DQ[41]/NC
MEM_MA_DATA40	CP48	DDR0_DQ[40]/NC
MEM_MA_DATA39	CP48	DDR0_DQ[39]/NC
MEM_MA_DATA38	DE39	DDR0_DQ[38]/NC
MEM_MA_DATA37	DD36	DDR0_DQ[37]/NC
MEM_MA_DATA36	DB36	DDR0_DQ[36]/NC
MEM_MA_DATA35	CP40	DDR0_DQ[35]/NC
MEM_MA_DATA34	DD30	DDR0_DQ[34]/NC
MEM_MA_DATA33	DE37	DDR0_DQ[33]/NC
MEM_MA_DATA32	DA37	DDR0_DQ[32]/NC
MEM_MA_DATA31	CR41	DDR0_DQ[31]/NC
MEM_MA_DATA30	DE18	DDR0_DQ[30]/NC
MEM_MA_DATA29	DB12	DDR0_DQ[29]/NC
MEM_MA_DATA28	DA13	DDR0_DQ[28]/NC
MEM_MA_DATA27	DD18	DDR0_DQ[27]/NC
MEM_MA_DATA26	DE16	DDR0_DQ[26]/NC
MEM_MA_DATA25	DE13	DDR0_DQ[25]/NC
MEM_MA_DATA24	DD12	DDR0_DQ[24]/NC
MEM_MA_DATA23	DE9	DDR0_DQ[23]/NC
MEM_MA_DATA22	DA9	DDR0_DQ[22]/NC
MEM_MA_DATA21	DD8	DDR0_DQ[21]/NC
MEM_MA_DATA20	DB6	DDR0_DQ[20]/NC
MEM_MA_DATA19	DD10	DDR0_DQ[19]/NC
MEM_MA_DATA18	DB10	DDR0_DQ[18]/NC
MEM_MA_DATA17	DE7	DDR0_DQ[17]/NC
MEM_MA_DATA16	DA7	DDR0_DQ[16]/NC
MEM_MA_DATA15	CV2	DDR0_DQ[15]/NC
MEM_MA_DATA14	CT2	DDR0_DQ[14]/NC
MEM_MA_DATA13	CN5	DDR0_DQ[13]/NC
MEM_MA_DATA12	CM4	DDR0_DQ[12]/NC
MEM_MA_DATA11	CW3	DDR0_DQ[11]/NC
MEM_MA_DATA10	CV4	DDR0_DQ[10]/NC
MEM_MA_DATA9	CN3	DDR0_DQ[9]/NC
MEM_MA_DATA8	CR5	DDR0_DQ[8]/NC
MEM_MA_DATA7	CG3	DDR0_DQ[7]/NC
MEM_MA_DATA6	CG3	DDR0_DQ[6]/NC
MEM_MA_DATA5	CC5	DDR0_DQ[5]/NC
MEM_MA_DATA4	CJ5	DDR0_DQ[4]/NC
MEM_MA_DATA3	CG5	DDR0_DQ[3]/NC
MEM_MA_DATA2	CC3	DDR0_DQ[2]/NC
MEM_MA_DATA1	CA3	DDR0_DQ[1]/NC
MEM_MA_CLK_H3	DE19	DDR0_ECC[7]/NC
MEM_MA_CLK_L3	DE21	DDR0_ECC[6]/NC
MEM_MA_CLK_H2	DE18	DDR0_ECC[5]/NC
MEM_MA_CLK_L2	CP18	DDR0_ECC[4]/NC
MEM_MA_CLK_H1	CP21	DDR0_ECC[3]/NC
MEM_MA_CLK_L1	CV20	DDR0_ECC[2]/NC
MEM_MA_CLK_H0	CW19	DDR0_ECC[1]/NC
MEM_MA_CLK_L0	CW19	DDR0_ECC[0]/NC
MEM_MA_BG_1	DB24	DDR0_BG[1]/NC
MEM_MA_BG_0	CT24	DDR0_BG[0]/NC
MEM_MA_BA_1	CD28	DDR0_BA[1]/NC
MEM_MA_BA_0	CU29	DDR0_BA[0]/NC

CPU1B

SKYLAKE-X

DDR0_DQ[63]/NC	DD18	DDR0_DQ[63]/NC
DDR0_DQ[62]/NC	DD18	DDR0_DQ[62]/NC
DDR0_DQ[61]/NC	DD50	DDR0_DQ[61]/NC
DDR0_DQ[60]/NC	DF50	DDR0_DQ[60]/NC
DDR0_DQ[59]/NC	CU47	DDR0_DQ[59]/NC
DDR0_DQ[58]/NC	CW47	DDR0_DQ[58]/NC
DDR0_DQ[57]/NC	DD44	DDR0_DQ[57]/NC
DDR0_DQ[56]/NC	DF44	DDR0_DQ[56]/NC
DDR0_DQ[55]/NC	DD38	DDR0_DQ[55]/NC
DDR0_DQ[54]/NC	DF38	DDR0_DQ[54]/NC
DDR0_DQ[53]/NC	CV14	DDR0_DQ[53]/NC
DDR0_DQ[52]/NC	DE14	DDR0_DQ[52]/NC
DDR0_DQ[51]/NC	CY8	DDR0_DQ[51]/NC
DDR0_DQ[50]/NC	DB8	DDR0_DQ[50]/NC
DDR0_DQ[49]/NC	CR3	DDR0_DQ[49]/NC
DDR0_DQ[48]/NC	CP2	DDR0_DQ[48]/NC
DDR0_DQ[47]/NC	CB4	DDR0_DQ[47]/NC
DDR0_DQ[46]/NC	CD4	DDR0_DQ[46]/NC
DDR0_DQ[45]/NC	DB20	DDR0_DQ[45]/NC
DDR0_DQ[44]/NC	DA21	DDR0_DQ[44]/NC
DDR0_DQ[43]/NC	CY50	DDR0_DQ[43]/NC
DDR0_DQ[42]/NC	DB50	DDR0_DQ[42]/NC
DDR0_DQ[41]/NC	CR47	DDR0_DQ[41]/NC
DDR0_DQ[40]/NC	CN47	DDR0_DQ[40]/NC
DDR0_DQ[39]/NC	CY44	DDR0_DQ[39]/NC
DDR0_DQ[38]/NC	DB44	DDR0_DQ[38]/NC
DDR0_DQ[37]/NC	DB38	DDR0_DQ[37]/NC
DDR0_DQ[36]/NC	CY38	DDR0_DQ[36]/NC
DDR0_DQ[35]/NC	DD14	DDR0_DQ[35]/NC
DDR0_DQ[34]/NC	DF14	DDR0_DQ[34]/NC
DDR0_DQ[33]/NC	DF8	DDR0_DQ[33]/NC
DDR0_DQ[32]/NC	DD8	DDR0_DQ[32]/NC
DDR0_DQ[31]/NC	CU5	DDR0_DQ[31]/NC
DDR0_DQ[30]/NC	CT4	DDR0_DQ[30]/NC
DDR0_DQ[29]/NC	CH4	DDR0_DQ[29]/NC
DDR0_DQ[28]/NC	CF4	DDR0_DQ[28]/NC
DDR0_DQ[27]/NC	CU33	DDR0_DQ[27]/NC
DDR0_DQ[26]/NC	DB30	DDR0_DQ[26]/NC
DDR0_DQ[25]/NC	CT30	DDR0_DQ[25]/NC
DDR0_DQ[24]/NC	DC31	DDR0_DQ[24]/NC
DDR0_DQ[23]/NC	CW31	DDR0_DQ[23]/NC
DDR0_DQ[22]/NC	DF24	DDR0_DQ[22]/NC
DDR0_DQ[21]/NC	CY24	DDR0_DQ[21]/NC
DDR0_DQ[20]/NC	CW29	DDR0_DQ[20]/NC
DDR0_DQ[19]/NC	DE25	DDR0_DQ[19]/NC
DDR0_DQ[18]/NC	DE25	DDR0_DQ[18]/NC
DDR0_DQ[17]/NC	CP22	DDR0_DQ[17]/NC
DDR0_DQ[16]/NC	CY26	DDR0_DQ[16]/NC
DDR0_DQ[15]/NC	CW26	DDR0_DQ[15]/NC
DDR0_DQ[14]/NC	DB26	DDR0_DQ[14]/NC
DDR0_DQ[13]/NC	CU25	DDR0_DQ[13]/NC
DDR0_DQ[12]/NC	CT26	DDR0_DQ[12]/NC
DDR0_DQ[11]/NC	DC27	DDR0_DQ[11]/NC
DDR0_DQ[10]/NC	CT28	DDR0_DQ[10]/NC
DDR0_DQ[9]/NC	DDC23	DDR0_DQ[9]/NC
DDR0_DQ[8]/NC	DE23	DDR0_DQ[8]/NC
DDR0_DQ[7]/NC	CU21	DDR0_DQ[7]/NC
DDR0_DQ[6]/NC	CT22	DDR0_DQ[6]/NC
DDR0_DQ[5]/NC	DE33	DDR0_DQ[5]/NC
DDR0_DQ[4]/NC	DB32	DDR0_DQ[4]/NC
DDR0_DQ[3]/NC	CW33	DDR0_DQ[3]/NC
DDR0_DQ[2]/NC	CU31	DDR0_DQ[2]/NC
DDR0_DQ[1]/NC	DE33	DDR0_DQ[1]/NC
DDR0_DQ[0]/NC	DB32	DDR0_DQ[0]/NC
DDR0_CS_N[7]/NC	DF34	DDR0_CS_N[7]/NC
DDR0_CS_N[6]/NC	DB34	DDR0_CS_N[6]/NC
DDR0_CS_N[5]/NC	CT32	DDR0_CS_N[5]/NC
DDR0_CS_N[4]/NC	DE31	DDR0_CS_N[4]/NC
DDR0_CS_N[3]/NC	CT34	DDR0_CS_N[3]/NC
DDR0_CS_N[2]/NC	CY34	DDR0_CS_N[2]/NC
DDR0_CS_N[1]/NC	CY32	DDR0_CS_N[1]/NC
DDR0_CS_N[0]/NC	CY30	DDR0_CS_N[0]/NC
DDR0_CID[2]/NC	DC33	DDR0_CID[2]/NC
DDR0_ACT_N/NC	CU23	DDR0_ACT_N/NC
DDR0_ALERT_N/NC	CW23	DDR0_ALERT_N/NC
DDR0_PAR/NC	DE29	DDR0_PAR/NC
DDR0_CAVREF/NC	CD20	DDR0_CAVREF/NC

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MEM\_MB\_DATA[63.0] <>> MEM\_MB\_DATA[63.0] 11

CPU1C		
SKYLAKE-X		
MEM_MB_DATA63	CE49	DDR1_DQ[63]/NC
MEM_MB_DATA62	CL49	DDR1_DQ[62]/NC
MEM_MB_DATA61	CM50	DDR1_DQ[61]/NC
MEM_MB_DATA60	CF48	DDR1_DQ[60]/NC
MEM_MB_DATA59	CH48	DDR1_DQ[59]/NC
MEM_MB_DATA58	CH48	DDR1_DQ[58]/NC
MEM_MB_DATA57	CL51	DDR1_DQ[57]/NC
MEM_MB_DATA56	CL51	DDR1_DQ[56]/NC
MEM_MB_DATA55	CK46	DDR1_DQ[55]/NC
MEM_MB_DATA54	CL45	DDR1_DQ[54]/NC
MEM_MB_DATA53	CL45	DDR1_DQ[53]/NC
MEM_MB_DATA52	CH42	DDR1_DQ[52]/NC
MEM_MB_DATA51	CG45	DDR1_DQ[51]/NC
MEM_MB_DATA50	CH46	DDR1_DQ[50]/NC
MEM_MB_DATA49	CL43	DDR1_DQ[49]/NC
MEM_MB_DATA48	CL43	DDR1_DQ[48]/NC
MEM_MB_DATA47	CH43	DDR1_DQ[47]/NC
MEM_MB_DATA46	CV42	DDR1_DQ[46]/NC
MEM_MB_DATA45	CP40	DDR1_DQ[45]/NC
MEM_MB_DATA44	CR49	DDR1_DQ[44]/NC
MEM_MB_DATA43	CR43	DDR1_DQ[43]/NC
MEM_MB_DATA42	CP42	DDR1_DQ[42]/NC
MEM_MB_DATA41	CV40	DDR1_DQ[41]/NC
MEM_MB_DATA40	CU39	DDR1_DQ[40]/NC
MEM_MB_DATA39	CR40	DDR1_DQ[39]/NC
MEM_MB_DATA38	CL37	DDR1_DQ[38]/NC
MEM_MB_DATA37	CG37	DDR1_DQ[37]/NC
MEM_MB_DATA36	CH36	DDR1_DQ[36]/NC
MEM_MB_DATA35	CH36	DDR1_DQ[35]/NC
MEM_MB_DATA34	CG39	DDR1_DQ[34]/NC
MEM_MB_DATA33	CL36	DDR1_DQ[33]/NC
MEM_MB_DATA32	CK36	DDR1_DQ[32]/NC
MEM_MB_DATA31	CO16	DDR1_DQ[31]/NC
MEM_MB_DATA30	CE15	DDR1_DQ[30]/NC
MEM_MB_DATA29	CA13	DDR1_DQ[29]/NC
MEM_MB_DATA28	CB12	DDR1_DQ[28]/NC
MEM_MB_DATA27	CB16	DDR1_DQ[27]/NC
MEM_MB_DATA26	CA15	DDR1_DQ[26]/NC
MEM_MB_DATA25	CE13	DDR1_DQ[25]/NC
MEM_MB_DATA24	CO12	DDR1_DQ[24]/NC
MEM_MB_DATA23	CT14	DDR1_DQ[23]/NC
MEM_MB_DATA22	CR13	DDR1_DQ[22]/NC
MEM_MB_DATA21	CR13	DDR1_DQ[21]/NC
MEM_MB_DATA20	CR15	DDR1_DQ[20]/NC
MEM_MB_DATA19	CR15	DDR1_DQ[19]/NC
MEM_MB_DATA18	CR15	DDR1_DQ[18]/NC
MEM_MB_DATA17	CK12	DDR1_DQ[17]/NC
MEM_MB_DATA16	CK12	DDR1_DQ[16]/NC
MEM_MB_DATA15	CP10	DDR1_DQ[15]/NC
MEM_MB_DATA14	CR9	DDR1_DQ[14]/NC
MEM_MB_DATA13	CH9	DDR1_DQ[13]/NC
MEM_MB_DATA12	CJ7	DDR1_DQ[12]/NC
MEM_MB_DATA11	CM10	DDR1_DQ[11]/NC
MEM_MB_DATA10	CL7	DDR1_DQ[10]/NC
MEM_MB_DATA9	CO7	DDR1_DQ[9]/NC
MEM_MB_DATA8	CG7	DDR1_DQ[8]/NC
MEM_MB_DATA7	CG9	DDR1_DQ[7]/NC
MEM_MB_DATA6	CF8	DDR1_DQ[6]/NC
MEM_MB_DATA5	BY8	DDR1_DQ[5]/NC
MEM_MB_DATA4	CA9	DDR1_DQ[4]/NC
MEM_MB_DATA3	CF10	DDR1_DQ[3]/NC
MEM_MB_DATA2	CO10	DDR1_DQ[2]/NC
MEM_MB_DATA1	CC7	DDR1_DQ[1]/NC
MEM_MB_CLK_H3	CK26	DDR1_CLK_DP[3]/NC
MEM_MB_CLK_L3	CL27	DDR1_CLK_DP[3]/NC
MEM_MB_CLK_H2	CH26	DDR1_CLK_DP[2]/NC
MEM_MB_CLK_L2	CL27	DDR1_CLK_DP[2]/NC
MEM_MB_CLK_H1	CH30	DDR1_CLK_DP[1]/NC
MEM_MB_CLK_L1	CG31	DDR1_CLK_DP[1]/NC
MEM_MB_CLK_H0	CH28	DDR1_CLK_DP[0]/NC
MEM_MB_CLK_L0	CG29	DDR1_CLK_DP[0]/NC
MEM_MB_BG_1	CE25	DDR1_BG[1]/NC
MEM_MB_BG_0	CD24	DDR1_BG[0]/NC
MEM_MB_BA_1	CK28	DDR1_BA[1]/NC
MEM_MB_BA_0	CL29	DDR1_BA[0]/NC

CPU1C

SKYLAKE-X

DDR1_DQ[63]/NC	CP18	DDR1_DQ[63]/NC
DDR1_DQ[62]/NC	CL18	DDR1_DQ[62]/NC
DDR1_DQ[61]/NC	CL49	DDR1_DQ[61]/NC
DDR1_DQ[60]/NC	CK48	DDR1_DQ[60]/NC
DDR1_DQ[59]/NC	CK48	DDR1_DQ[59]/NC
DDR1_DQ[58]/NC	CL45	DDR1_DQ[58]/NC
DDR1_DQ[57]/NC	CL45	DDR1_DQ[57]/NC
DDR1_DQ[56]/NC	CK46	DDR1_DQ[56]/NC
DDR1_DQ[55]/NC	CL45	DDR1_DQ[55]/NC
DDR1_DQ[54]/NC	CL45	DDR1_DQ[54]/NC
DDR1_DQ[53]/NC	CL45	DDR1_DQ[53]/NC
DDR1_DQ[52]/NC	CL45	DDR1_DQ[52]/NC
DDR1_DQ[51]/NC	CL15	DDR1_DQ[51]/NC
DDR1_DQ[50]/NC	CL15	DDR1_DQ[50]/NC
DDR1_DQ[49]/NC	CK48	DDR1_DQ[49]/NC
DDR1_DQ[48]/NC	CK48	DDR1_DQ[48]/NC
DDR1_DQ[47]/NC	CK48	DDR1_DQ[47]/NC
DDR1_DQ[46]/NC	CK48	DDR1_DQ[46]/NC
DDR1_DQ[45]/NC	CK48	DDR1_DQ[45]/NC
DDR1_DQ[44]/NC	CK48	DDR1_DQ[44]/NC
DDR1_DQ[43]/NC	CK48	DDR1_DQ[43]/NC
DDR1_DQ[42]/NC	CK48	DDR1_DQ[42]/NC
DDR1_DQ[41]/NC	CK48	DDR1_DQ[41]/NC
DDR1_DQ[40]/NC	CK48	DDR1_DQ[40]/NC
DDR1_DQ[39]/NC	CK48	DDR1_DQ[39]/NC
DDR1_DQ[38]/NC	CK48	DDR1_DQ[38]/NC
DDR1_DQ[37]/NC	CK48	DDR1_DQ[37]/NC
DDR1_DQ[36]/NC	CK48	DDR1_DQ[36]/NC
DDR1_DQ[35]/NC	CK48	DDR1_DQ[35]/NC
DDR1_DQ[34]/NC	CK48	DDR1_DQ[34]/NC
DDR1_DQ[33]/NC	CK48	DDR1_DQ[33]/NC
DDR1_DQ[32]/NC	CK48	DDR1_DQ[32]/NC
DDR1_DQ[31]/NC	CK48	DDR1_DQ[31]/NC
DDR1_DQ[30]/NC	CK48	DDR1_DQ[30]/NC
DDR1_DQ[29]/NC	CK48	DDR1_DQ[29]/NC
DDR1_DQ[28]/NC	CK48	DDR1_DQ[28]/NC
DDR1_DQ[27]/NC	CK48	DDR1_DQ[27]/NC
DDR1_DQ[26]/NC	CK48	DDR1_DQ[26]/NC
DDR1_DQ[25]/NC	CK48	DDR1_DQ[25]/NC
DDR1_DQ[24]/NC	CK48	DDR1_DQ[24]/NC
DDR1_DQ[23]/NC	CK48	DDR1_DQ[23]/NC
DDR1_DQ[22]/NC	CK48	DDR1_DQ[22]/NC
DDR1_DQ[21]/NC	CK48	DDR1_DQ[21]/NC
DDR1_DQ[20]/NC	CK48	DDR1_DQ[20]/NC
DDR1_DQ[19]/NC	CK48	DDR1_DQ[19]/NC
DDR1_DQ[18]/NC	CK48	DDR1_DQ[18]/NC
DDR1_DQ[17]/NC	CK48	DDR1_DQ[17]/NC
DDR1_DQ[16]/NC	CK48	DDR1_DQ[16]/NC
DDR1_DQ[15]/NC	CK48	DDR1_DQ[15]/NC
DDR1_DQ[14]/NC	CK48	DDR1_DQ[14]/NC
DDR1_DQ[13]/NC	CK48	DDR1_DQ[13]/NC
DDR1_DQ[12]/NC	CK48	DDR1_DQ[12]/NC
DDR1_DQ[11]/NC	CK48	DDR1_DQ[11]/NC
DDR1_DQ[10]/NC	CK48	DDR1_DQ[10]/NC
DDR1_DQ[9]/NC	CK48	DDR1_DQ[9]/NC
DDR1_DQ[8]/NC	CK48	DDR1_DQ[8]/NC
DDR1_DQ[7]/NC	CK48	DDR1_DQ[7]/NC
DDR1_DQ[6]/NC	CK48	DDR1_DQ[6]/NC
DDR1_DQ[5]/NC	CK48	DDR1_DQ[5]/NC
DDR1_DQ[4]/NC	CK48	DDR1_DQ[4]/NC
DDR1_DQ[3]/NC	CK48	DDR1_DQ[3]/NC
DDR1_DQ[2]/NC	CK48	DDR1_DQ[2]/NC
DDR1_DQ[1]/NC	CK48	DDR1_DQ[1]/NC
DDR1_DQ[0]/NC	CK48	DDR1_DQ[0]/NC
DDR1_CS_N[7]/NC	CP34	DDR1_CS_N[7]/NC
DDR1_CS_N[6]/NC	CP34	DDR1_CS_N[6]/NC
DDR1_CS_N[5]/NC	CP34	DDR1_CS_N[5]/NC
DDR1_CS_N[4]/NC	CP34	DDR1_CS_N[4]/NC
DDR1_CS_N[3]/NC	CP34	DDR1_CS_N[3]/NC
DDR1_CS_N[2]/NC	CP34	DDR1_CS_N[2]/NC
DDR1_CS_N[1]/NC	CP34	DDR1_CS_N[1]/NC
DDR1_CS_N[0]/NC	CP34	DDR1_CS_N[0]/NC
DDR1_CID[2]/NC	CK34	DDR1_CID[2]/NC
DDR1_ACT_N/NC	CH22	DDR1_ACT_N/NC
DDR1_ALERT_N/NC	CK22	DDR1_ALERT_N/NC
DDR1_PAR/NC	CH22	DDR1_PAR/NC
DDR1_CAVREF/NC	CH20	DDR1_CAVREF/NC

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MEM\_MC\_DATA[63..0] <>> MEM\_MC\_DATA[63..0] 12

CPU1D SKYLAKE-X

MEM\_MC\_DATA63 N47  
MEM\_MC\_DATA62 M48  
MEM\_MC\_DATA61 J45  
MEM\_MC\_DATA60 K44  
MEM\_MC\_DATA59 J47  
MEM\_MC\_DATA58 K48  
MEM\_MC\_DATA57 N45  
MEM\_MC\_DATA56 M44  
MEM\_MC\_DATA55 C51  
MEM\_MC\_DATA54 B50  
MEM\_MC\_DATA53 E47  
MEM\_MC\_DATA52 C47  
MEM\_MC\_DATA51 F50  
MEM\_MC\_DATA50 E51  
MEM\_MC\_DATA49 B48  
MEM\_MC\_DATA48 F48  
MEM\_MC\_DATA47 F44  
MEM\_MC\_DATA46 B44  
MEM\_MC\_DATA45 F42  
MEM\_MC\_DATA44 E41  
MEM\_MC\_DATA43 D43  
MEM\_MC\_DATA42 E45  
MEM\_MC\_DATA41 B42  
MEM\_MC\_DATA40 C41  
MEM\_MC\_DATA39 C39  
MEM\_MC\_DATA38 B38  
MEM\_MC\_DATA37 E35  
MEM\_MC\_DATA36 C35  
MEM\_MC\_DATA35 F38  
MEM\_MC\_DATA34 B36  
MEM\_MC\_DATA33 B36  
MEM\_MC\_DATA32 F36  
MEM\_MC\_DATA31 C15  
MEM\_MC\_DATA30 B14  
MEM\_MC\_DATA29 F12  
MEM\_MC\_DATA28 E11  
MEM\_MC\_DATA27 E15  
MEM\_MC\_DATA26 F14  
MEM\_MC\_DATA25 B12  
MEM\_MC\_DATA24 C11  
MEM\_MC\_DATA23 F8  
MEM\_MC\_DATA22 B8  
MEM\_MC\_DATA21 E5  
MEM\_MC\_DATA20 F6  
MEM\_MC\_DATA19 C9  
MEM\_MC\_DATA18 E9  
MEM\_MC\_DATA17 B6  
MEM\_MC\_DATA16 C5  
MEM\_MC\_DATA15 H2  
MEM\_MC\_DATA14 K2  
MEM\_MC\_DATA13 T4  
MEM\_MC\_DATA12 V4  
MEM\_MC\_DATA11 H4  
MEM\_MC\_DATA10 K4  
MEM\_MC\_DATA9 T2  
MEM\_MC\_DATA8 V2  
MEM\_MC\_DATA7 A4  
MEM\_MC\_DATA6 A4  
MEM\_MC\_DATA5 A3  
MEM\_MC\_DATA4 A2  
MEM\_MC\_DATA3 A2  
MEM\_MC\_DATA2 A2  
MEM\_MC\_DATA1 A1  
MEM\_MC\_DATA0 A1

DDR3\_DQS\_DP[17] G19  
DDR3\_DQS\_DP[16] E19  
DDR3\_DQS\_DP[15] H46  
DDR3\_DQS\_DP[14] C49  
DDR3\_DQS\_DP[13] A49  
DDR3\_DQS\_DP[12] G43  
DDR3\_DQS\_DP[11] C37  
DDR3\_DQS\_DP[10] A37  
DDR3\_DQS\_DP[9] G13  
DDR3\_DQS\_DP[8] E13  
DDR3\_DQS\_DP[7] E7  
DDR3\_DQS\_DP[6] R3  
DDR3\_DQS\_DP[5] F4  
DDR3\_DQS\_DP[4] A4  
DDR3\_DQS\_DP[3] A3  
DDR3\_DQS\_DP[2] C18  
DDR3\_DQS\_DP[1] A19  
DDR3\_DQS\_DP[0] M46

MEM\_MC\_DQS\_H7 <>> MEM\_MC\_DQS\_H7 12  
MEM\_MC\_DQS\_L7 <>> MEM\_MC\_DQS\_L7 12  
MEM\_MC\_DQS\_H6 <>> MEM\_MC\_DQS\_H6 12  
MEM\_MC\_DQS\_L6 <>> MEM\_MC\_DQS\_L6 12  
MEM\_MC\_DQS\_H5 <>> MEM\_MC\_DQS\_H5 12  
MEM\_MC\_DQS\_L5 <>> MEM\_MC\_DQS\_L5 12  
MEM\_MC\_DQS\_H4 <>> MEM\_MC\_DQS\_H4 12  
MEM\_MC\_DQS\_L4 <>> MEM\_MC\_DQS\_L4 12  
MEM\_MC\_DQS\_H3 <>> MEM\_MC\_DQS\_H3 12  
MEM\_MC\_DQS\_L3 <>> MEM\_MC\_DQS\_L3 12  
MEM\_MC\_DQS\_H2 <>> MEM\_MC\_DQS\_H2 12  
MEM\_MC\_DQS\_L2 <>> MEM\_MC\_DQS\_L2 12  
MEM\_MC\_DQS\_H1 <>> MEM\_MC\_DQS\_H1 12  
MEM\_MC\_DQS\_L1 <>> MEM\_MC\_DQS\_L1 12  
MEM\_MC\_DQS\_H0 <>> MEM\_MC\_DQS\_H0 12  
MEM\_MC\_DQS\_L0 <>> MEM\_MC\_DQS\_L0 12

DDR3\_MA[17] G33  
DDR3\_MA[16] E31  
DDR3\_MA[15] D32  
DDR3\_MA[14] G31  
DDR3\_MA[13] K32  
DDR3\_MA[12] C23  
DDR3\_MA[11] B24  
DDR3\_MA[10] K30  
DDR3\_MA[9] A23  
DDR3\_MA[8] D24  
DDR3\_MA[7] E23  
DDR3\_MA[6] A25  
DDR3\_MA[5] B26  
DDR3\_MA[4] L25  
DDR3\_MA[3] K26  
DDR3\_MA[2] G27  
DDR3\_MA[1] H26  
DDR3\_MA[0] B30

MEM\_MC\_ADD[17..0] <>> MEM\_MC\_ADD[17..0] 12

MEM\_MC\_ADD17 G33  
MEM\_MC\_ADD16 E31  
MEM\_MC\_ADD15 D32  
MEM\_MC\_ADD14 G31  
MEM\_MC\_ADD13 K32  
MEM\_MC\_ADD12 C23  
MEM\_MC\_ADD11 B24  
MEM\_MC\_ADD10 K30  
MEM\_MC\_ADD9 A23  
MEM\_MC\_ADD8 D24  
MEM\_MC\_ADD7 E23  
MEM\_MC\_ADD6 A25  
MEM\_MC\_ADD5 B26  
MEM\_MC\_ADD4 L25  
MEM\_MC\_ADD3 K26  
MEM\_MC\_ADD2 G27  
MEM\_MC\_ADD1 H26  
MEM\_MC\_ADD0 B30

DDR3\_CKE[3] L21  
DDR3\_CKE[2] K22  
DDR3\_CKE[1] H22  
DDR3\_CKE[0] L23

MEM\_MC\_CKE3 <>> MEM\_MC\_CKE3 12  
MEM\_MC\_CKE2 <>> MEM\_MC\_CKE2 12  
MEM\_MC\_CKE1 <>> MEM\_MC\_CKE1 12  
MEM\_MC\_CKE0 <>> MEM\_MC\_CKE0 12

DDR3\_ODT[3] B34  
DDR3\_ODT[2] E33  
DDR3\_ODT[1] K34  
DDR3\_ODT[0] L31

MEM\_MC\_ODT3 <>> MEM\_MC\_ODT3 12  
MEM\_MC\_ODT2 <>> MEM\_MC\_ODT2 12  
MEM\_MC\_ODT1 <>> MEM\_MC\_ODT1 12  
MEM\_MC\_ODT0 <>> MEM\_MC\_ODT0 12

DDR3\_CS\_N[7] F34  
DDR3\_CS\_N[6] H34  
DDR3\_CS\_N[5] A33  
DDR3\_CS\_N[4] B32  
DDR3\_CS\_N[3] H34  
DDR3\_CS\_N[2] H32  
DDR3\_CS\_N[1] H30  
DDR3\_CS\_N[0] H30

MEM\_MC\_CS\_L7 <>> MEM\_MC\_CS\_L7 12  
MEM\_MC\_CS\_L6 <>> MEM\_MC\_CS\_L6 12  
MEM\_MC\_CS\_L5 <>> MEM\_MC\_CS\_L5 12  
MEM\_MC\_CS\_L4 <>> MEM\_MC\_CS\_L4 12  
MEM\_MC\_CS\_L3 <>> MEM\_MC\_CS\_L3 12  
MEM\_MC\_CS\_L2 <>> MEM\_MC\_CS\_L2 12  
MEM\_MC\_CS\_L1 <>> MEM\_MC\_CS\_L1 12  
MEM\_MC\_CS\_L0 <>> MEM\_MC\_CS\_L0 12

DDR3\_CID[2] L33

MEM\_MC\_C2 <>> MEM\_MC\_C2 12

DDR3\_ACT\_N R21  
DDR3\_ALERT\_N R21  
DDR3\_PAR R21

MEM\_MC\_ACT\_N <>> MEM\_MC\_ACT\_N 12  
MEM\_MC\_ALERT\_N <>> MEM\_MC\_ALERT\_N 12  
MEM\_MC\_PAR <>> MEM\_MC\_PAR 12

DDR3\_CAVREF R21

VREF\_CPU\_DDR2

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MEM\_MD\_DATA[63..0] <>> MEM\_MD\_DATA[63..0] 13

CPU1E SKYLAKE-X

MEM\_MD\_DATA63 T48  
MEM\_MD\_DATA62 U47  
MEM\_MD\_DATA61 AB48  
MEM\_MD\_DATA60 AC47  
MEM\_MD\_DATA59 U49  
MEM\_MD\_DATA58 W49  
MEM\_MD\_DATA57 V46  
MEM\_MD\_DATA56 AB48  
MEM\_MD\_DATA55 AB42  
MEM\_MD\_DATA54 AA43  
MEM\_MD\_DATA53 T42  
MEM\_MD\_DATA52 R43  
MEM\_MD\_DATA51 AA41  
MEM\_MD\_DATA50 W41  
MEM\_MD\_DATA49 T44  
MEM\_MD\_DATA48 V44  
MEM\_MD\_DATA47 K42  
MEM\_MD\_DATA46 J41  
MEM\_MD\_DATA45 N39  
MEM\_MD\_DATA44 M38  
MEM\_MD\_DATA43 M41  
MEM\_MD\_DATA42 M42  
MEM\_MD\_DATA41 J39  
MEM\_MD\_DATA40 K38  
MEM\_MD\_DATA39 AA39  
MEM\_MD\_DATA38 W39  
MEM\_MD\_DATA37 T36  
MEM\_MD\_DATA36 V36  
MEM\_MD\_DATA35 AB38  
MEM\_MD\_DATA34 AA37  
MEM\_MD\_DATA33 R37  
MEM\_MD\_DATA32 P36  
MEM\_MD\_DATA31 AA21  
MEM\_MD\_DATA30 AB20  
MEM\_MD\_DATA29 V46  
MEM\_MD\_DATA28 W15  
MEM\_MD\_DATA27 W21  
MEM\_MD\_DATA26 V20  
MEM\_MD\_DATA25 W17  
MEM\_MD\_DATA24 AA17  
MEM\_MD\_DATA23 L11  
MEM\_MD\_DATA22 N11  
MEM\_MD\_DATA21 P14  
MEM\_MD\_DATA20 T14  
MEM\_MD\_DATA19 K12  
MEM\_MD\_DATA18 L13  
MEM\_MD\_DATA17 T12  
MEM\_MD\_DATA16 U13  
MEM\_MD\_DATA15 L9  
MEM\_MD\_DATA14 K8  
MEM\_MD\_DATA13 U7  
MEM\_MD\_DATA12 T6  
MEM\_MD\_DATA11 R9  
MEM\_MD\_DATA10 N9  
MEM\_MD\_DATA9 M6  
MEM\_MD\_DATA8 P6  
MEM\_MD\_DATA7 Y8  
MEM\_MD\_DATA6 AA7  
MEM\_MD\_DATA5 AG7  
MEM\_MD\_DATA4 AF8  
MEM\_MD\_DATA3 AA9  
MEM\_MD\_DATA2 AC9  
MEM\_MD\_DATA1 AD6  
MEM\_MD\_DATA0 AF6

DDR4\_DQS\_DP[17] P16  
DDR4\_DQS\_DP[16] N17  
DDR4\_DQS\_DP[15] AA48  
DDR4\_DQS\_DP[14] Y46  
DDR4\_DQS\_DP[13] W43  
DDR4\_DQS\_DP[12] Y44  
DDR4\_DQS\_DP[11] K40  
DDR4\_DQS\_DP[10] H46  
DDR4\_DQS\_DP[9] Y36  
DDR4\_DQS\_DP[8] W37  
DDR4\_DQS\_DP[7] AB18  
DDR4\_DQS\_DP[6] AC19  
DDR4\_DQS\_DP[5] N15  
DDR4\_DQS\_DP[4] M14  
DDR4\_DQS\_DP[3] N7  
DDR4\_DQS\_DP[2] L7  
DDR4\_DQS\_DP[1] AC7  
DDR4\_DQS\_DP[0] AB6

MEM\_MD\_DQS\_H7 <>> MEM\_MD\_DQS\_H7 13  
MEM\_MD\_DQS\_L7 <>> MEM\_MD\_DQS\_L7 13  
MEM\_MD\_DQS\_H6 <>> MEM\_MD\_DQS\_H6 13  
MEM\_MD\_DQS\_L6 <>> MEM\_MD\_DQS\_L6 13  
MEM\_MD\_DQS\_H5 <>> MEM\_MD\_DQS\_H5 13  
MEM\_MD\_DQS\_L5 <>> MEM\_MD\_DQS\_L5 13  
MEM\_MD\_DQS\_H4 <>> MEM\_MD\_DQS\_H4 13  
MEM\_MD\_DQS\_L4 <>> MEM\_MD\_DQS\_L4 13  
MEM\_MD\_DQS\_H3 <>> MEM\_MD\_DQS\_H3 13  
MEM\_MD\_DQS\_L3 <>> MEM\_MD\_DQS\_L3 13  
MEM\_MD\_DQS\_H2 <>> MEM\_MD\_DQS\_H2 13  
MEM\_MD\_DQS\_L2 <>> MEM\_MD\_DQS\_L2 13  
MEM\_MD\_DQS\_H1 <>> MEM\_MD\_DQS\_H1 13  
MEM\_MD\_DQS\_L1 <>> MEM\_MD\_DQS\_L1 13  
MEM\_MD\_DQS\_H0 <>> MEM\_MD\_DQS\_H0 13  
MEM\_MD\_DQS\_L0 <>> MEM\_MD\_DQS\_L0 13

DDR4\_MA[17] U33  
DDR4\_MA[16] T30  
DDR4\_MA[15] P32  
DDR4\_MA[14] AB30  
DDR4\_MA[13] Y32  
DDR4\_MA[12] T24  
DDR4\_MA[11] P26  
DDR4\_MA[10] Y30  
DDR4\_MA[9] U25  
DDR4\_MA[8] Y24  
DDR4\_MA[7] N27  
DDR4\_MA[6] AB24  
DDR4\_MA[5] T26  
DDR4\_MA[4] AC25  
DDR4\_MA[3] W25  
DDR4\_MA[2] U27  
DDR4\_MA[1] Y26  
DDR4\_MA[0] AB28

MEM\_MD\_ADD[17..0] <>> MEM\_MD\_ADD[17..0] 13

MEM\_MD\_ADD17 U33  
MEM\_MD\_ADD16 T30  
MEM\_MD\_ADD15 P32  
MEM\_MD\_ADD14 AB30  
MEM\_MD\_ADD13 Y32  
MEM\_MD\_ADD12 T24  
MEM\_MD\_ADD11 P26  
MEM\_MD\_ADD10 Y30  
MEM\_MD\_ADD9 U25  
MEM\_MD\_ADD8 Y24  
MEM\_MD\_ADD7 N27  
MEM\_MD\_ADD6 AB24  
MEM\_MD\_ADD5 T26  
MEM\_MD\_ADD4 AC25  
MEM\_MD\_ADD3 W25  
MEM\_MD\_ADD2 U27  
MEM\_MD\_ADD1 Y26  
MEM\_MD\_ADD0 AB28

DDR4\_CKE[3] N21  
DDR4\_CKE[2] P22  
DDR4\_CKE[1] W23  
DDR4\_CKE[0] N23

MEM\_MD\_CKE3 <>> MEM\_MD\_CKE3 13  
MEM\_MD\_CKE2 <>> MEM\_MD\_CKE2 13  
MEM\_MD\_CKE1 <>> MEM\_MD\_CKE1 13  
MEM\_MD\_CKE0 <>> MEM\_MD\_CKE0 13

DDR4\_ODT[3] T34  
DDR4\_ODT[2] U31  
DDR4\_ODT[1] AC33  
DDR4\_ODT[0] AC31

MEM\_MD\_ODT3 <>> MEM\_MD\_ODT3 13  
MEM\_MD\_ODT2 <>> MEM\_MD\_ODT2 13  
MEM\_MD\_ODT1 <>> MEM\_MD\_ODT1 13  
MEM\_MD\_ODT0 <>> MEM\_MD\_ODT0 13

DDR4\_CS\_N[7] V34  
DDR4\_CS\_N[6] Y34  
DDR4\_CS\_N[5] T32  
DDR4\_CS\_N[4] N31  
DDR4\_CS\_N[3] AB34  
DDR4\_CS\_N[2] AC35  
DDR4\_CS\_N[1] W33  
DDR4\_CS\_N[0] AC29

MEM\_MD\_CS\_L7 <>> MEM\_MD\_CS\_L7 13  
MEM\_MD\_CS\_L6 <>> MEM\_MD\_CS\_L6 13  
MEM\_MD\_CS\_L5 <>> MEM\_MD\_CS\_L5 13  
MEM\_MD\_CS\_L4 <>> MEM\_MD\_CS\_L4 13  
MEM\_MD\_CS\_L3 <>> MEM\_MD\_CS\_L3 13  
MEM\_MD\_CS\_L2 <>> MEM\_MD\_CS\_L2 13  
MEM\_MD\_CS\_L1 <>> MEM\_MD\_CS\_L1 13  
MEM\_MD\_CS\_L0 <>> MEM\_MD\_CS\_L0 13

DDR4\_CID[2] AB32

MEM\_MD\_C2 <>> MEM\_MD\_C2 13

DDR4\_ACT\_N T22  
DDR4\_ALERT\_N N25  
DDR4\_PAR W31

MEM\_MD\_ACT\_N <>> MEM\_MD\_ACT\_N 13  
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DDR4\_CAVREF AA23

VREF\_CPU\_DDR3

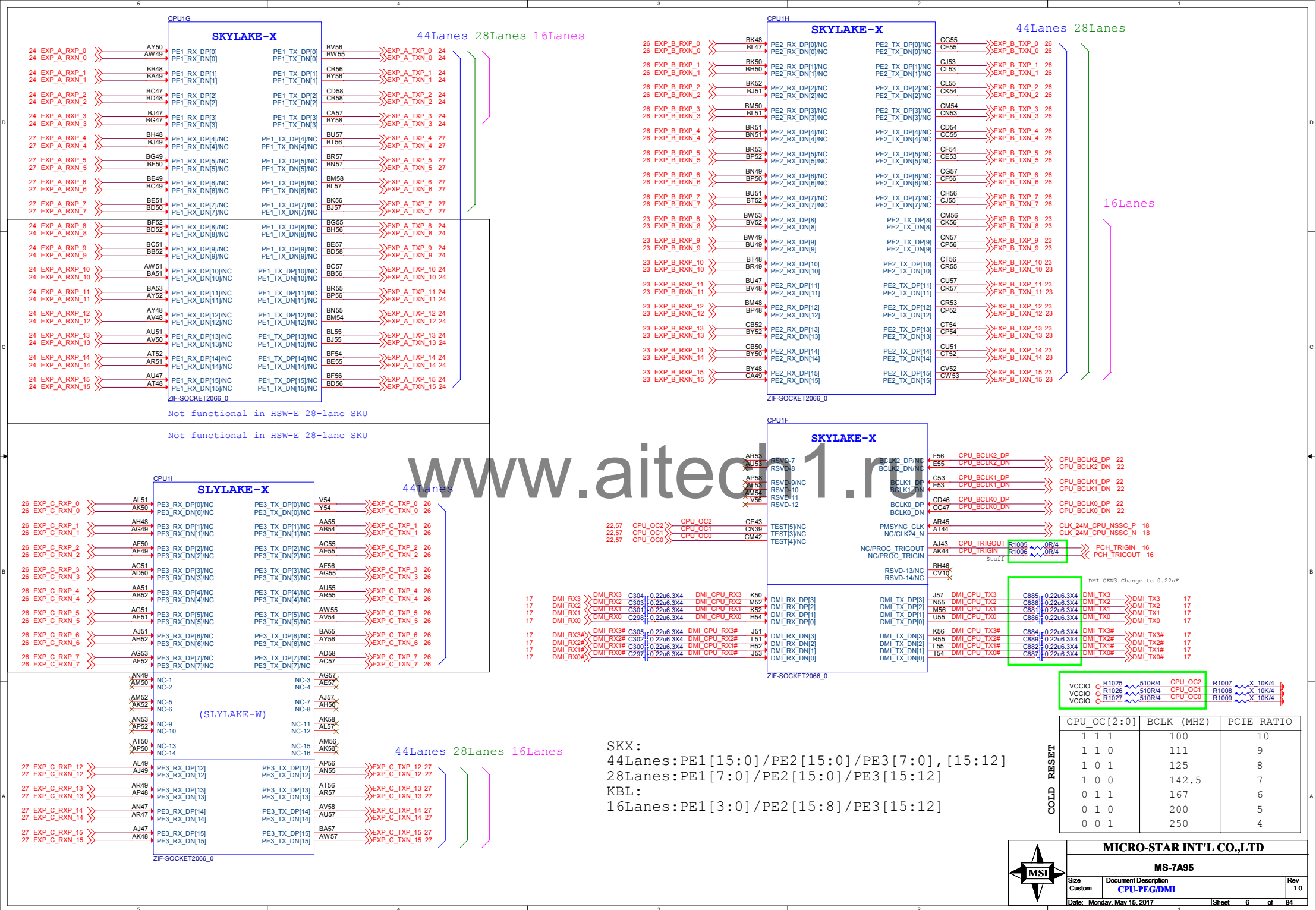
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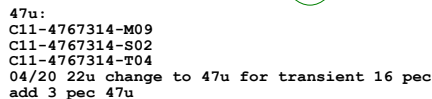
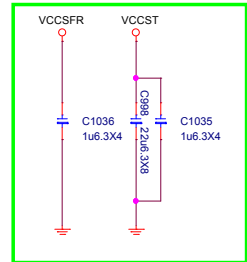
MICRO-STAR INT'L CO.,LTD

MS-7A95

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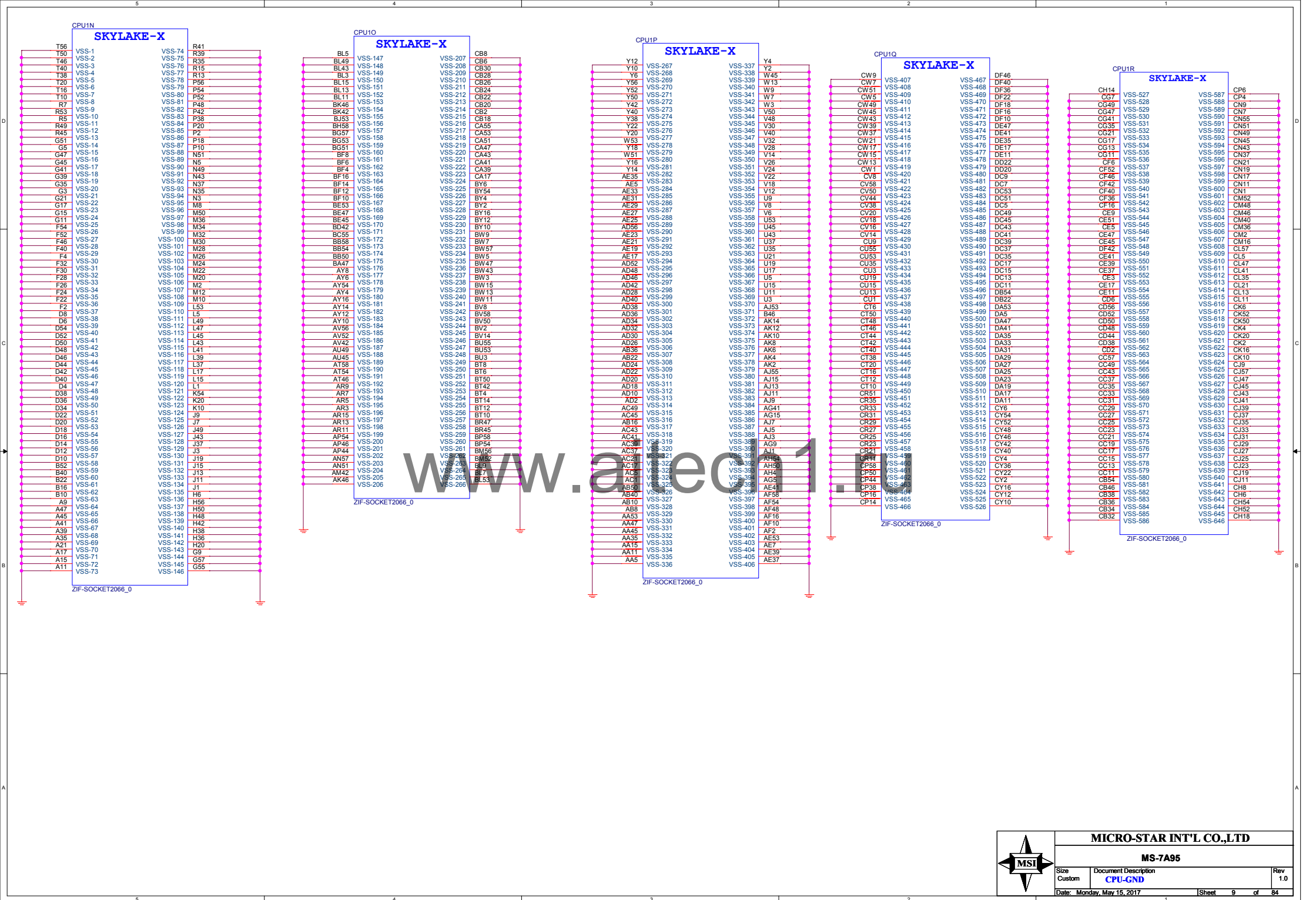






<b>MICRO-STAR INT'L CO.,LTD</b>			
<b>MS-7A95</b>			
Size Custom	Document Description <b>CPU-Power</b>		Rev 1.0
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MS-7A95

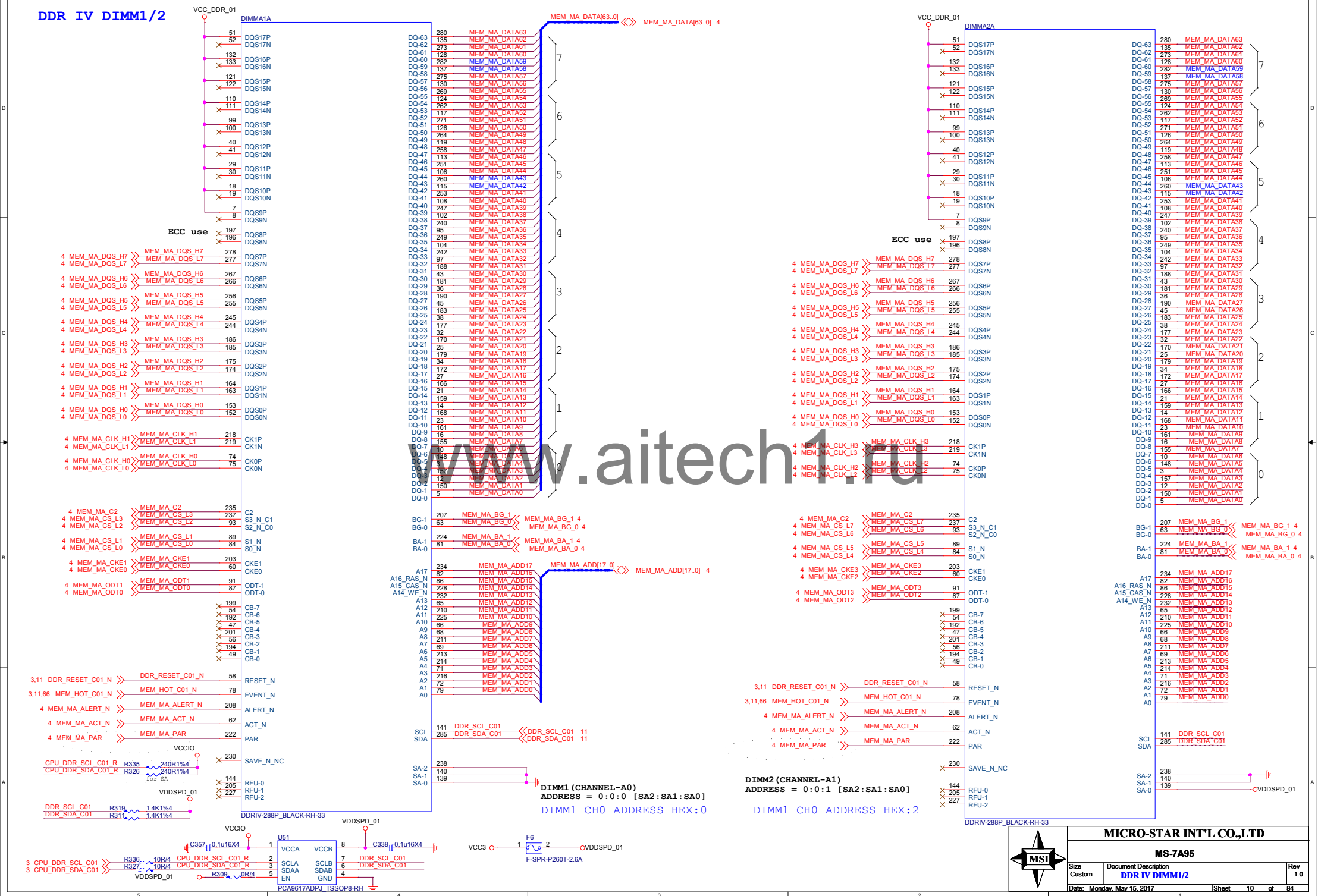
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Document Description
<b>CPU-GND</b>

Rev	1.0
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## DDR IV DIMM1/2



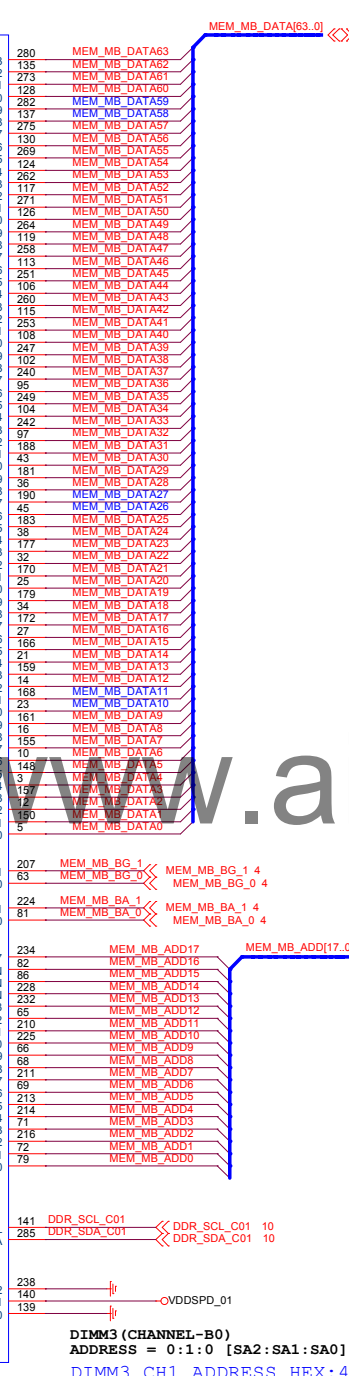
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MS-7A95

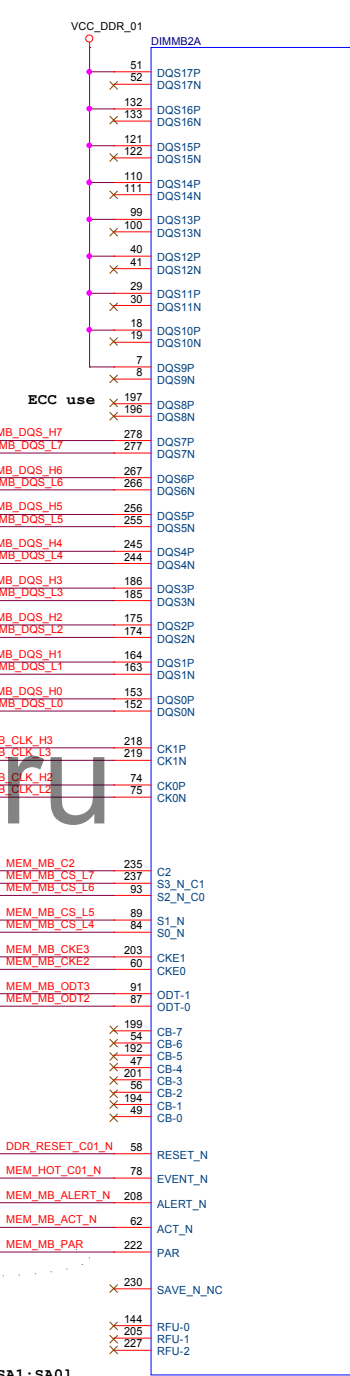
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VCC\_DDR\_01



DO-9	16	MEM_MB_DATA8			
DO-8	155	MEM_MB_DATA7	4 MEM_MB_CLK_H3	MEM_MB_CLK_H3	
DO-7	10	MEM_MB_DATA6	4 MEM_MB_CLK_L3	MEM_MB_CLK_L3	
DO-6	148	MEM_MB_DATA5			
DO-5	3	MEM_MB_DATA4			
DO-4	157	MEM_MB_DATA3	4 MEM_MB_CLK_H2	MEM_MB_CLK_H2	
DO-3	12	MEM_MB_DATA2	4 MEM_MB_CLK_L2	MEM_MB_CLK_L2	
DO-2	150	MEM_MB_DATA1			
DO-1	5	MEM_MB_DATA0			



VCC\_DDR\_01

DIMMB2A

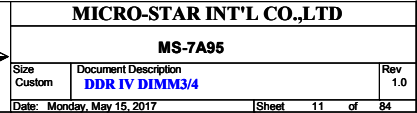
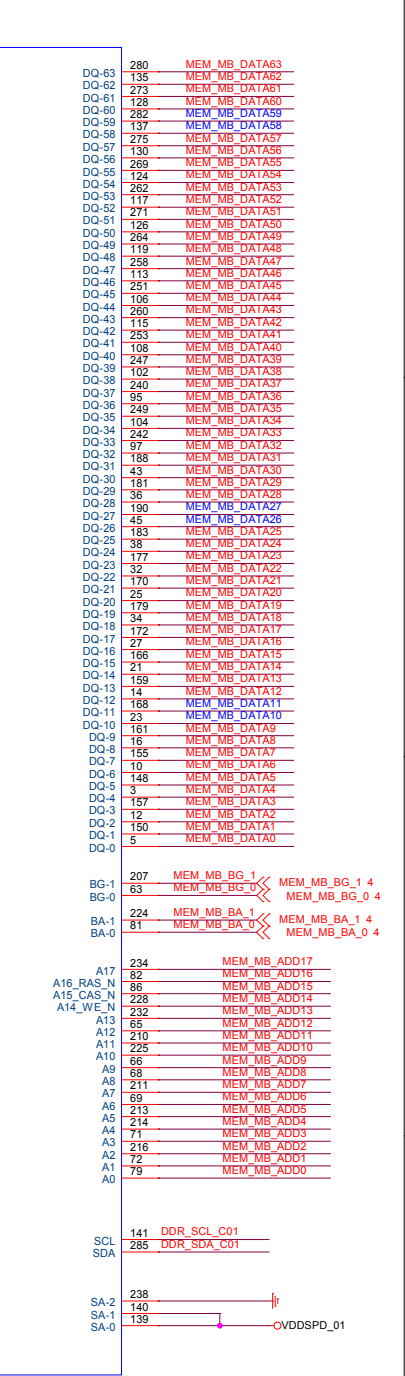
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DQS17P  
DQS17N  
DQS16P  
DQS16N  
DQS15P  
DQS15N  
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DQS0N  
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CK1N  
CK0P  
CK0N  
C2  
S3\_N\_C1  
S2\_N\_C0  
S1\_N  
S0\_N  
CKE1  
CKE0  
ODT-1  
ODT-0  
CB-7  
CB-6  
CB-5  
CB-4  
CB-3  
CB-2  
CB-1  
CB-0  
RESET\_N  
EVENT\_N  
ALERT\_N  
ACT\_N  
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RFU-1  
RFU-2

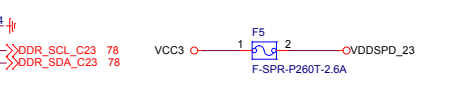
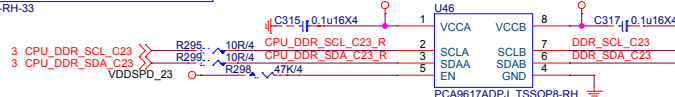
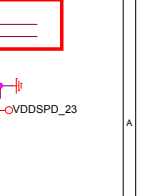
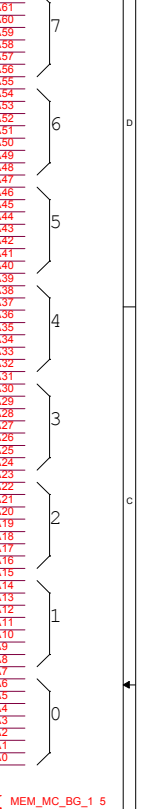
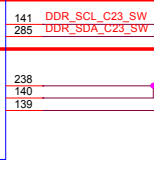
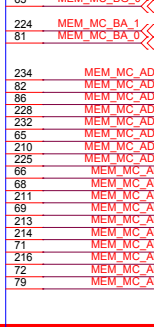
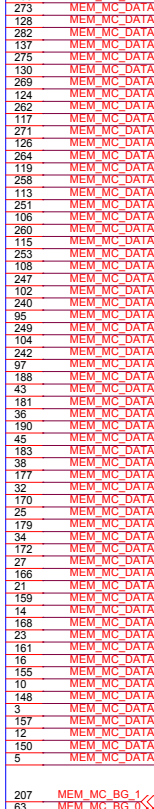
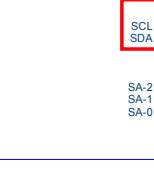
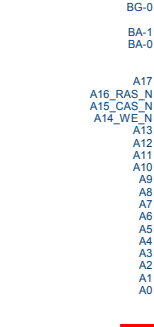
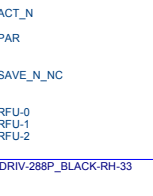
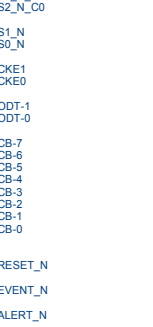
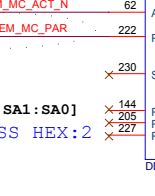
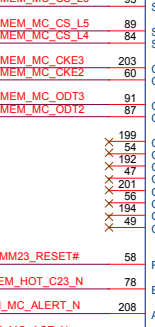
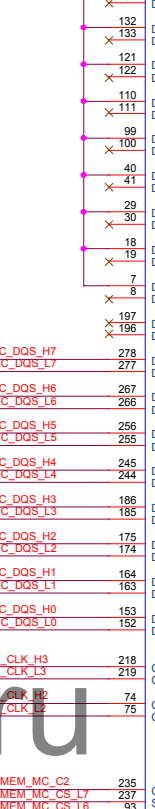
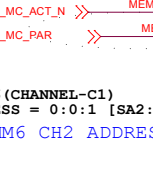
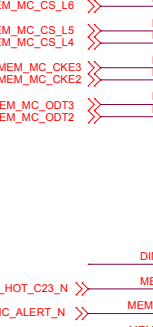
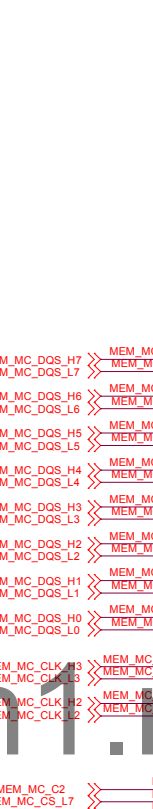
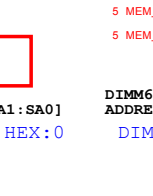
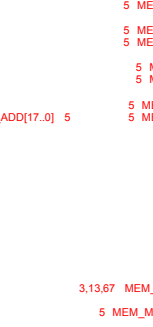
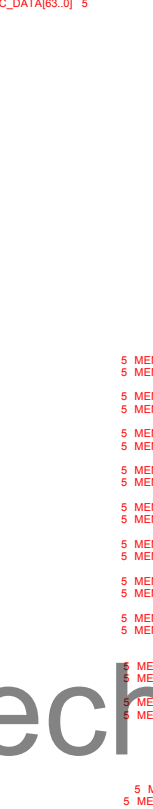
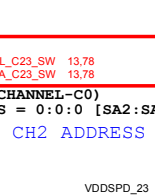
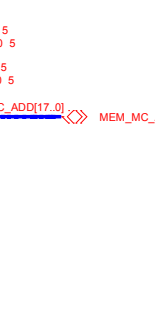
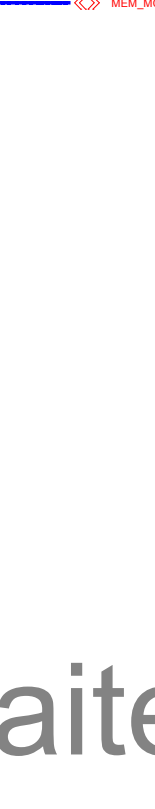
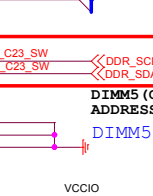
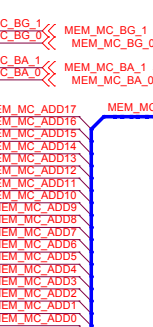
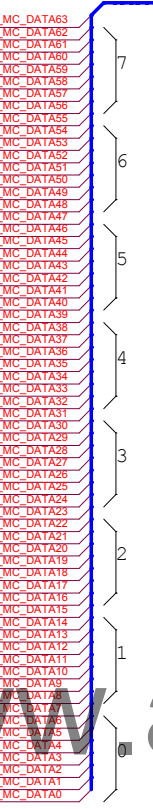
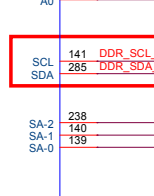
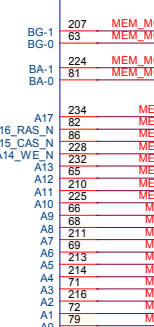
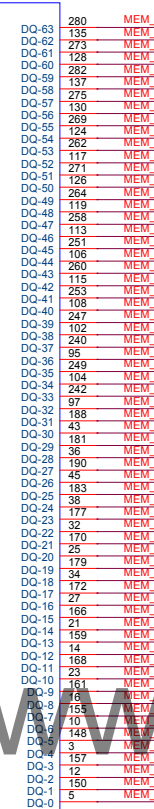
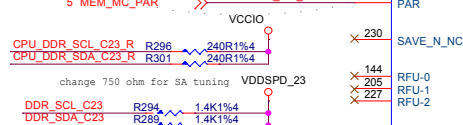
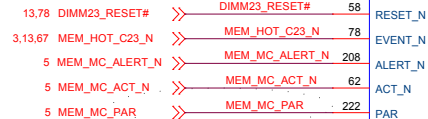
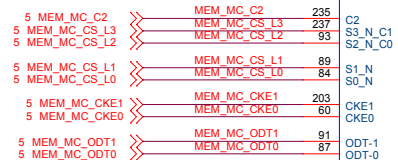
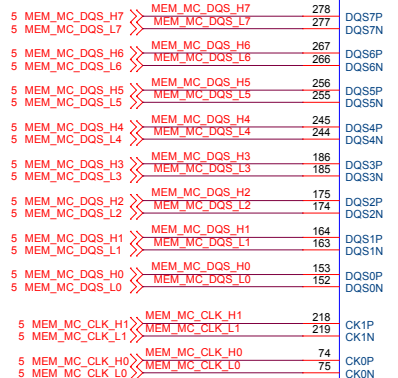
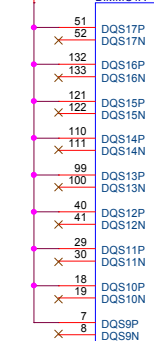
MB\_DQS\_H7  
MB\_DQS\_L7  
MB\_DQS\_H6  
MB\_DQS\_L6  
MB\_DQS\_H5  
MB\_DQS\_L5  
MB\_DQS\_H4  
MB\_DQS\_L4  
MB\_DQS\_H3  
MB\_DQS\_L3  
MB\_DQS\_H2  
MB\_DQS\_L2  
MB\_DQS\_H1  
MB\_DQS\_L1  
MB\_DQS\_H0  
MB\_DQS\_L0  
B\_CLK\_H3  
B\_CLK\_L3  
B\_CLK\_H2  
B\_CLK\_L2  
MEM\_MB\_C2  
MEM\_MB\_CS\_L7  
MEM\_MB\_CS\_L6  
MEM\_MB\_CS\_L5  
MEM\_MB\_CS\_L4  
MEM\_MB\_CKE3  
MEM\_MB\_CKE2  
MEM\_MB\_ODT3  
MEM\_MB\_ODT2  
DDR\_RESET\_C01\_N  
MEM\_HOT\_C01\_N  
MEM\_MB\_ALERT\_N  
MEM\_MB\_ACT\_N  
MEM\_MB\_PAR

ECC use

SA1-S901



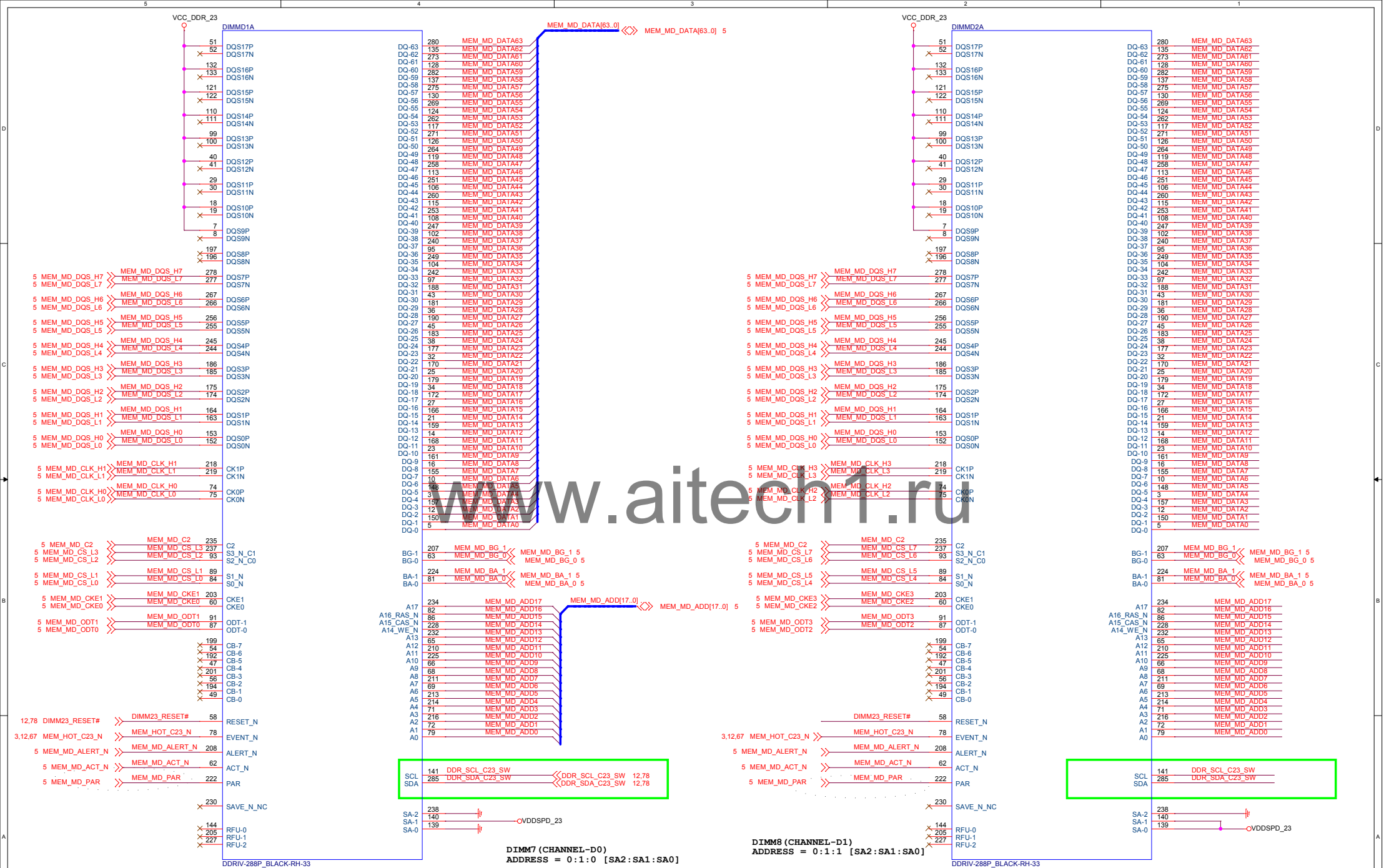
VCC\_DDR\_23



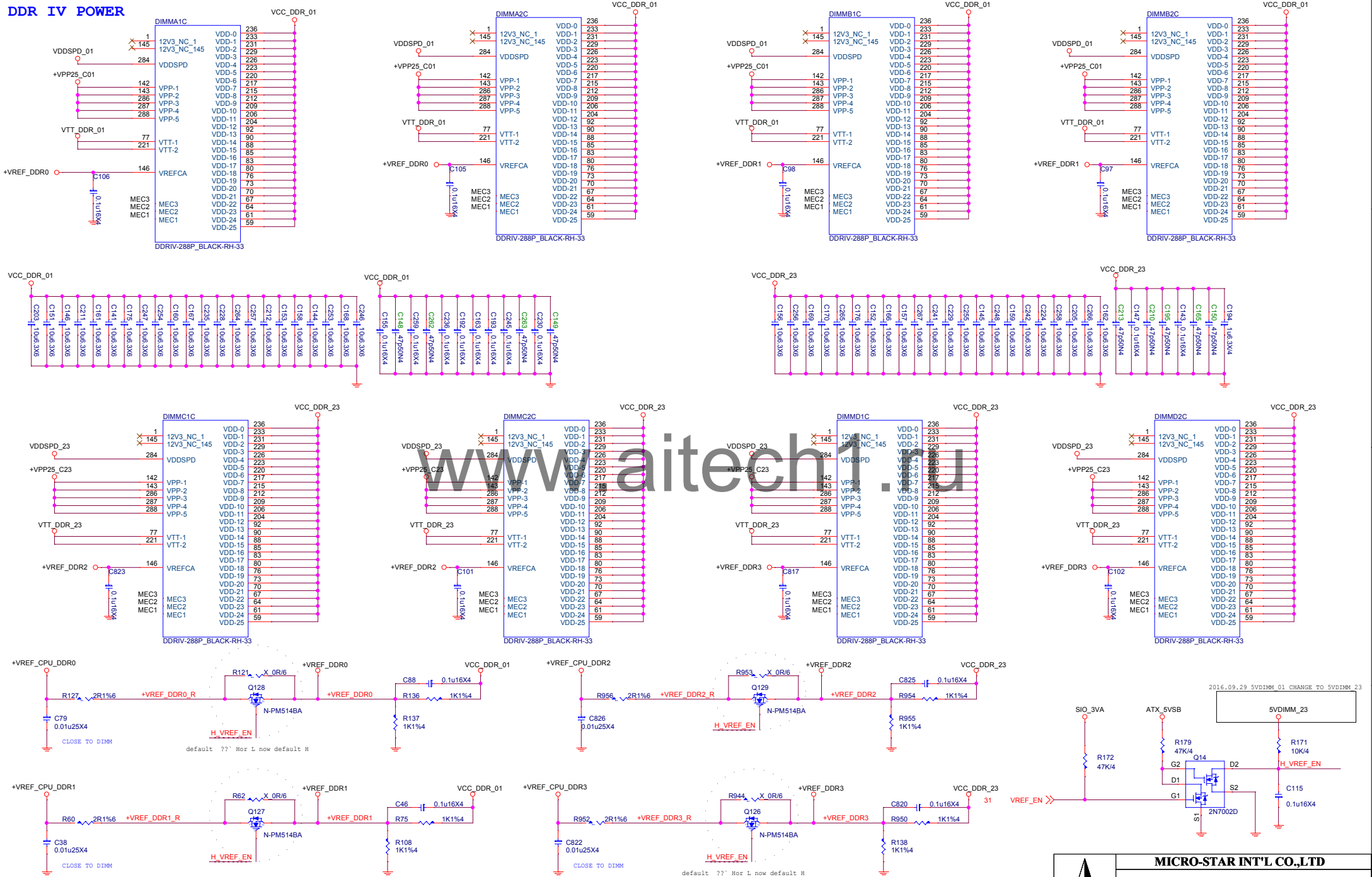
**MICRO-STAR INT'L CO.,LTD**

**MS-7A95**

Size Custom	Document Description <b>DDR IV DIMM5/6</b>	Rev 1.0
Date: Monday, May 15, 2017		Sheet 12 of 84



## DDR IV POWER

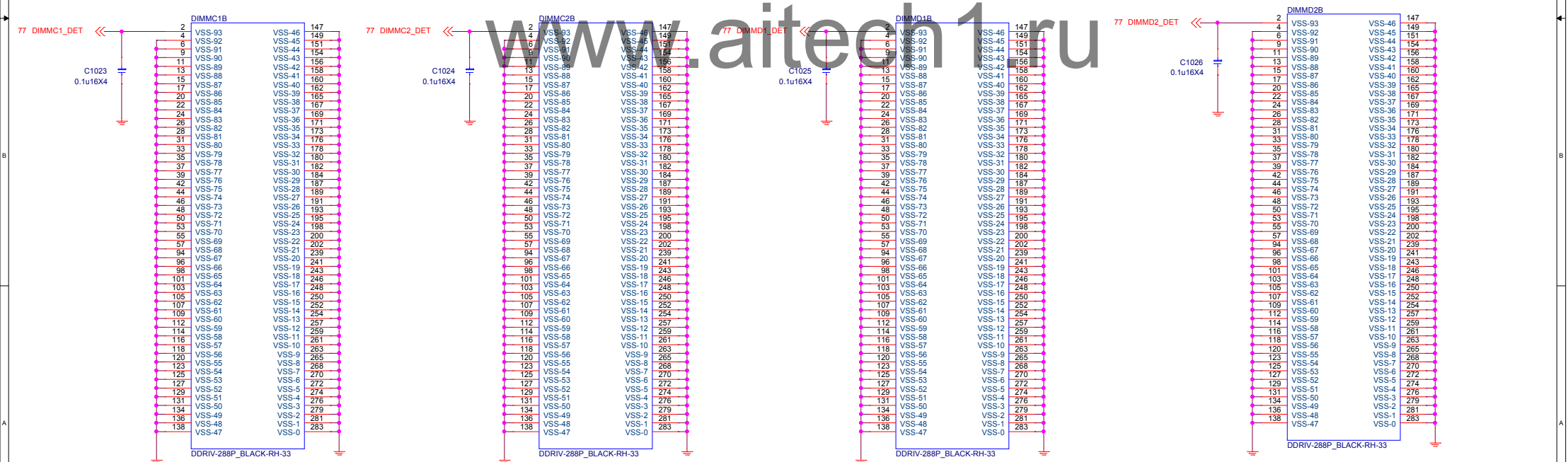
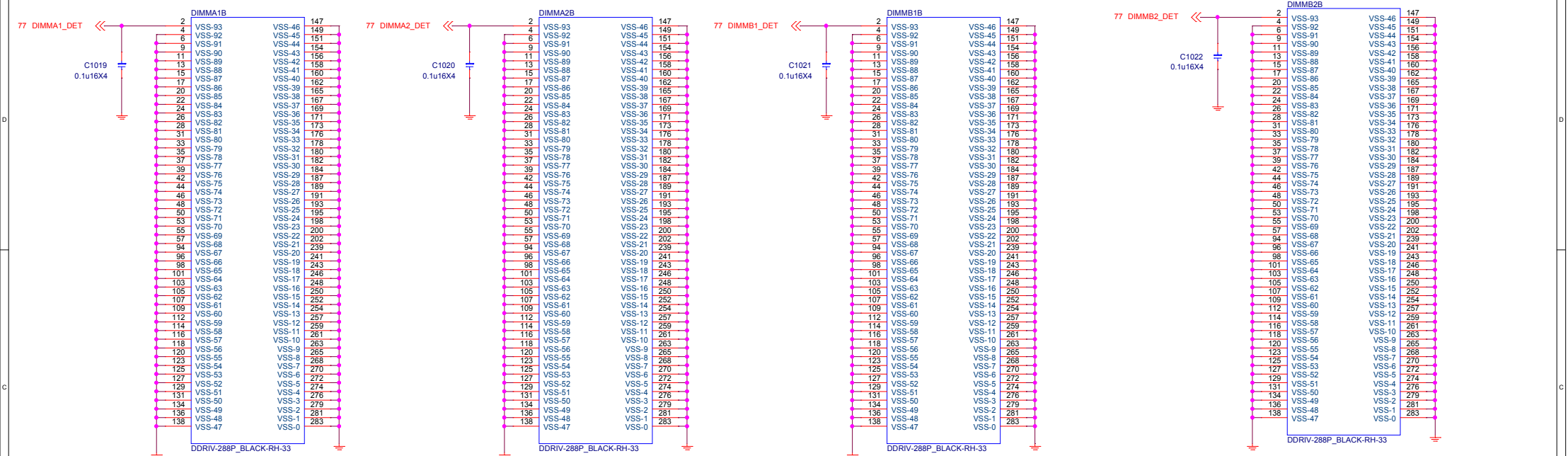


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Size Custom	Document Description <b>DDR IV POWER</b>	Rev 1.0
Date: Monday, May 15, 2017	Sheet 14 of 84	

## DDR IV GND



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## DDR IV GND

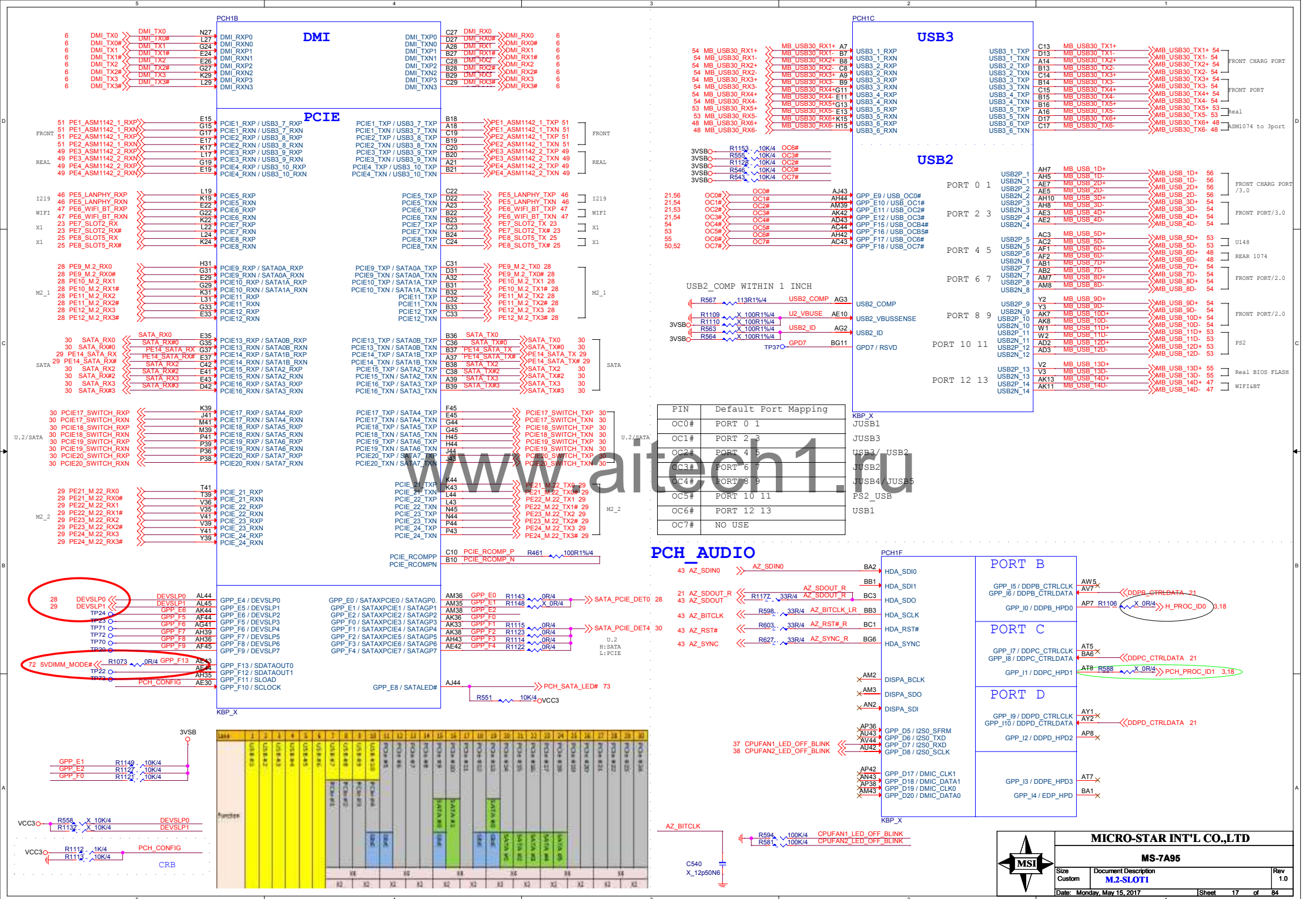
Rev	
1.0	

Date: Monday, May 15, 2017	Sheet 15 of 84
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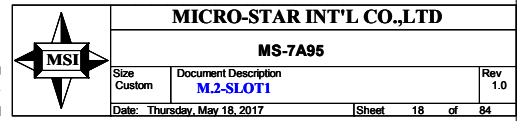


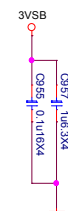
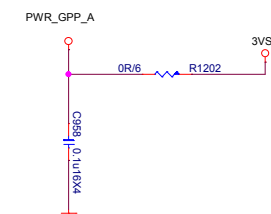
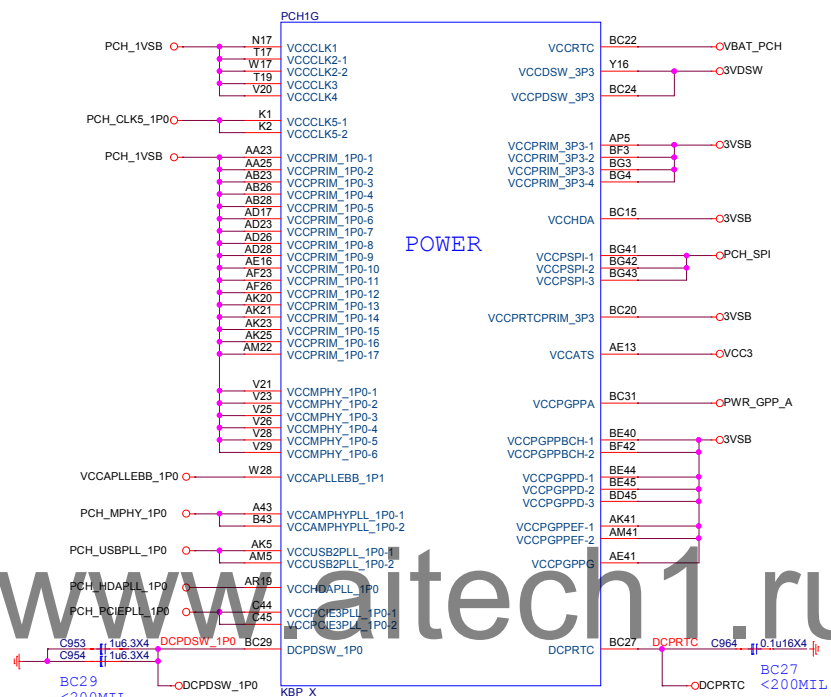
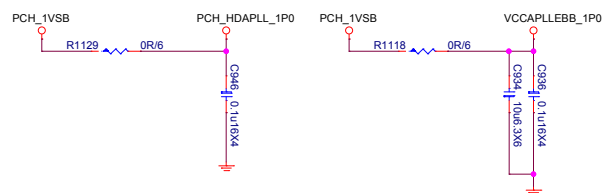






Used ESPI (GPPA) GPIO Group A will be come 1.8V level





POWER



**MICRO-STAR INT'L CO.,LTD**

**MS-7A95**


Size	Custom
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Document Description	<b>M.2-SLOT1</b>
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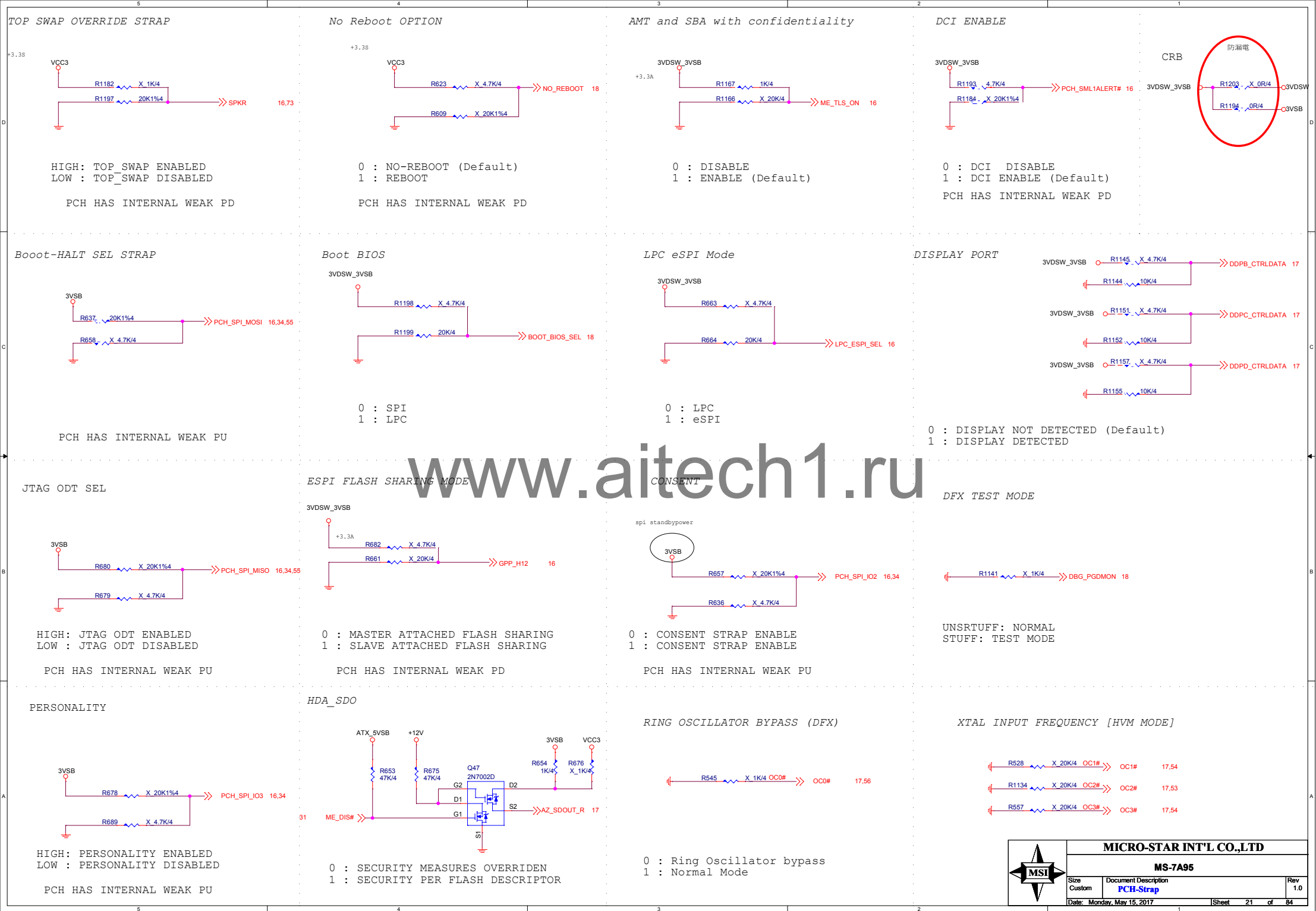
Rev	1.0
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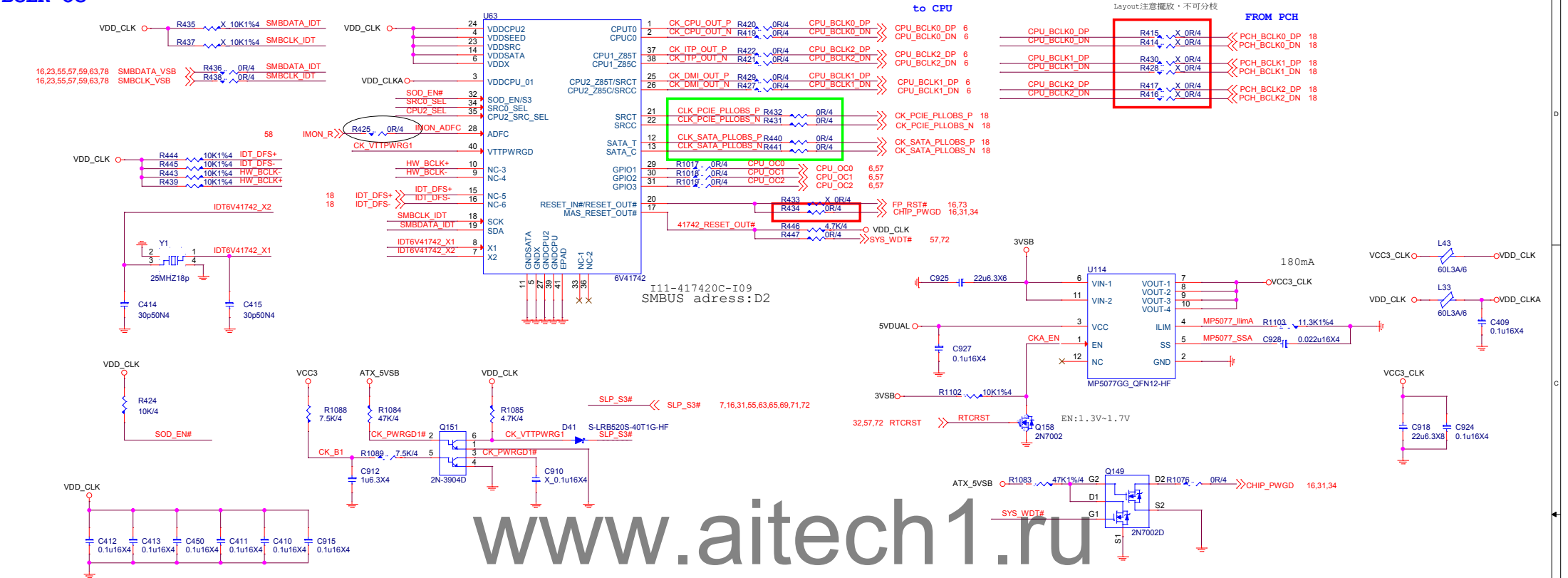
Date: Monday, May 15, 2017	Sheet 19 of 84
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MS-7A95		
Size	Document Description	Rev
Custom	M.2-SLOT1	1.0
Date: Monday, May 15, 2017		Sheet 20 of 84





3,27,31,59,63,65,67,78,79 H\_PROC\_ID1

CPU2\_SEL

H\_PROC\_ID1

SRC0\_SEL

VDD\_CLK

R412 4.7K/4

R423 4.7K/4

SRC0\_SEL

VDD\_CLK

R401 4.7K/4

R426 4.7K/4

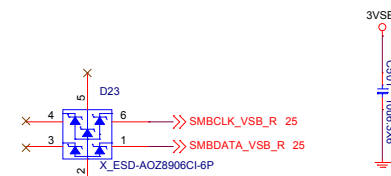
CPU2\_SEL

SRC0_SEL	Description	CPU	H_PROC_ID1
0	Source from CPUPLL	SKX	1
1	Source from PCIEPLL	KBX	0

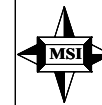
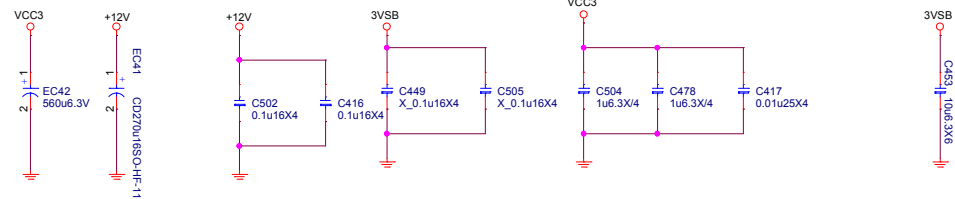
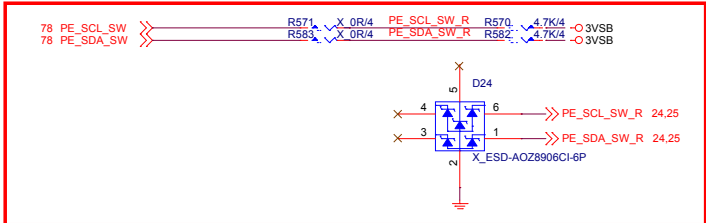
  

CPU2_SRC_SEL	Description	CPU	H_PROC_ID1
0	Source from CPUPLL	SKX	1
1	Source from PCIEPLL	KBX	0



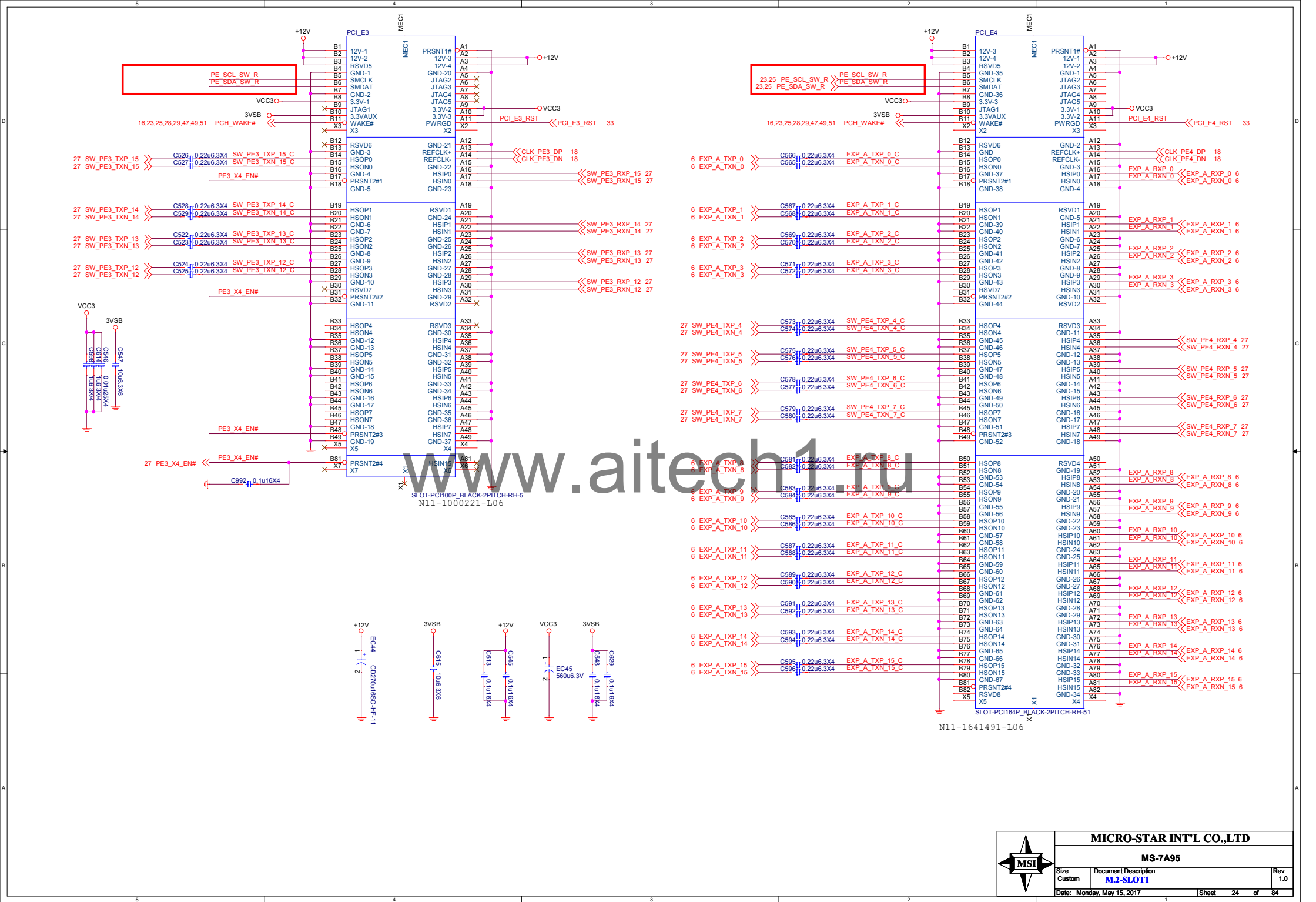


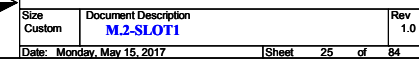
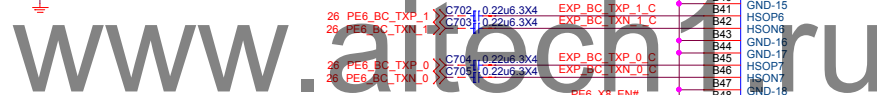
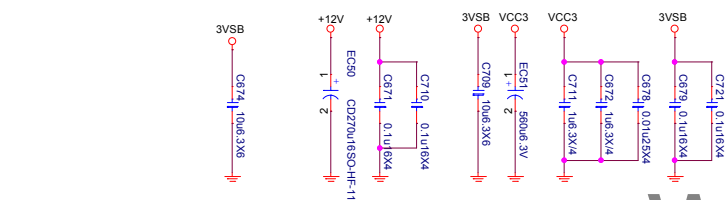
47 EXP\_B\_RXP 8 EXP\_B\_RXP 8 6  
48 EXP\_B\_RXN 8 EXP\_B\_RXN 8 6  
49  
50  
51  
52 PE1\_B\_RXP 7 PE1\_B\_RXP 7 26  
53 PE1\_B\_RXN 7  
SMBUS ESD

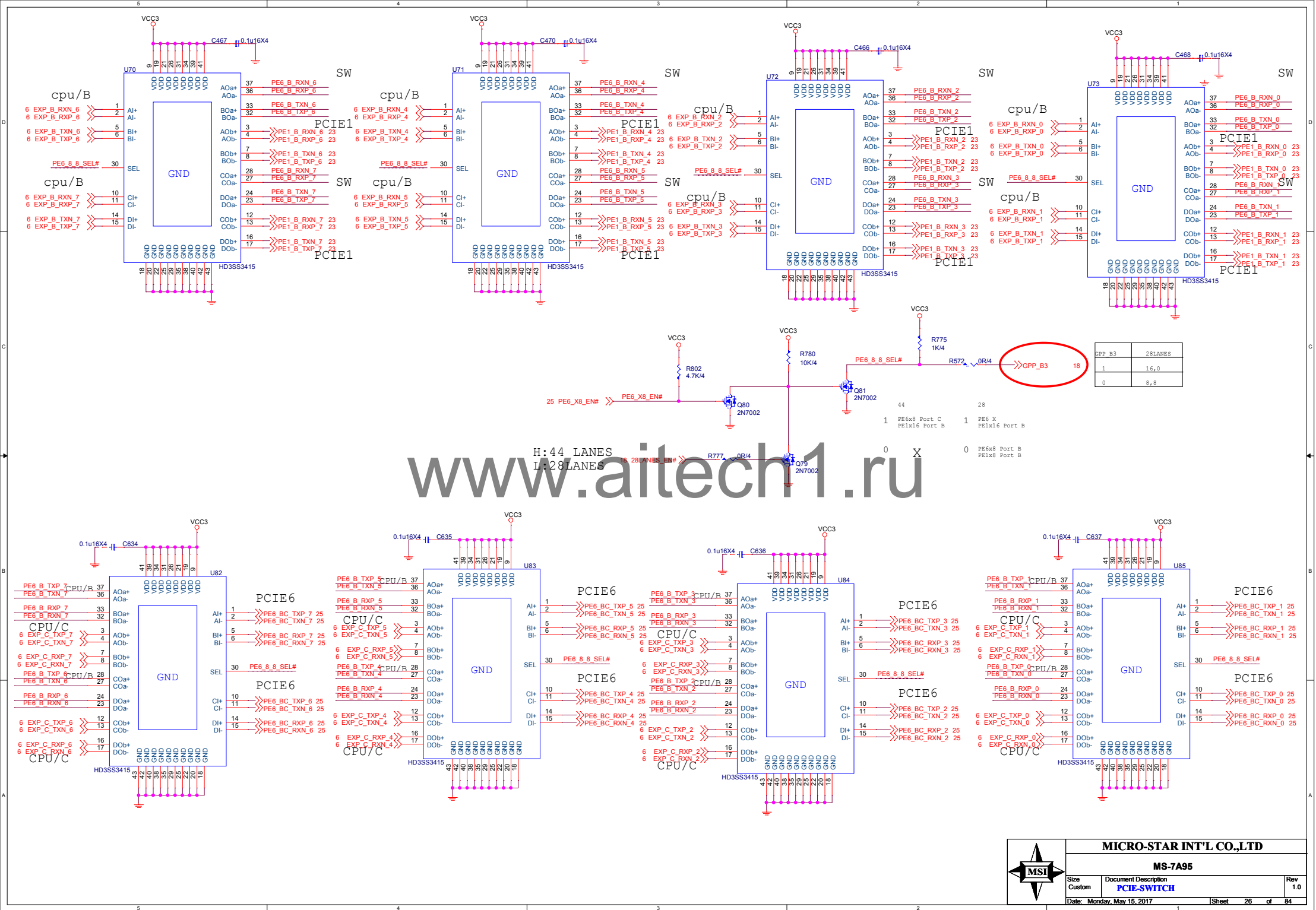


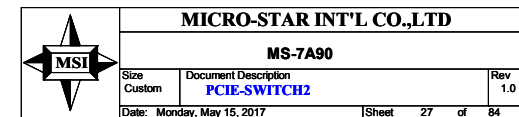
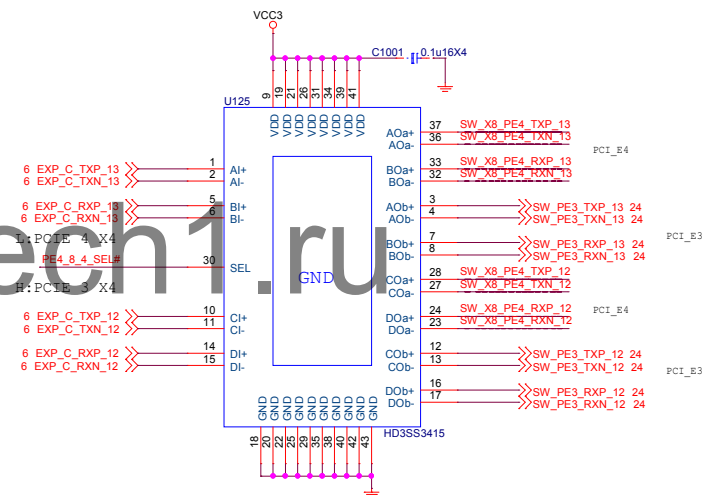
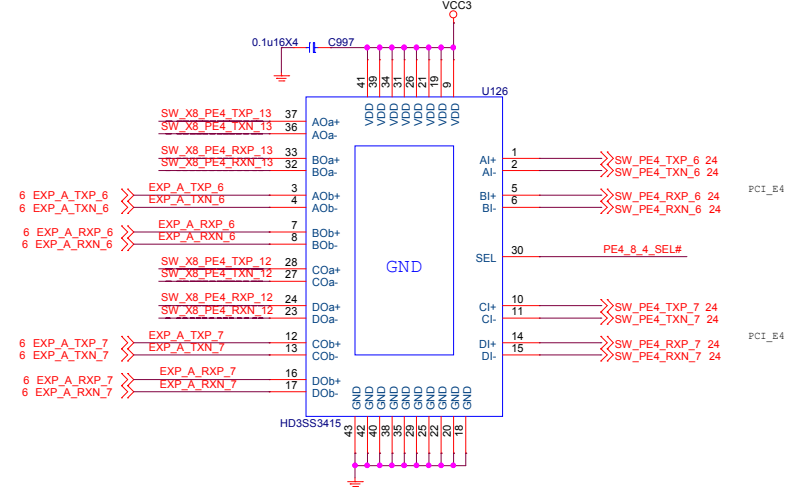
MS-7A95

Size Custom	Document Description <b>PCIE1(X16) &amp; PCIE2(X1) Slots</b>	Rev 1.0
Date: Monday, May 15, 2017	Sheet 23 of 84	

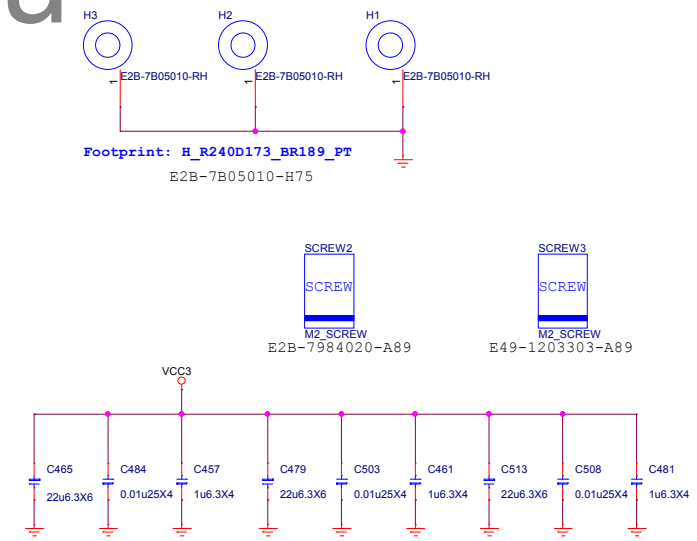
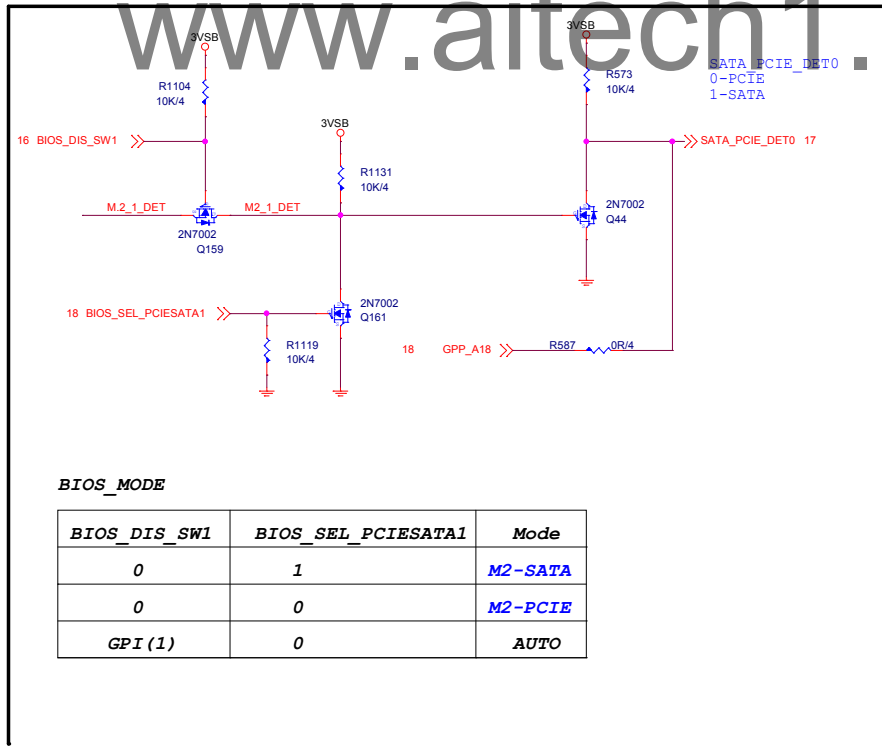
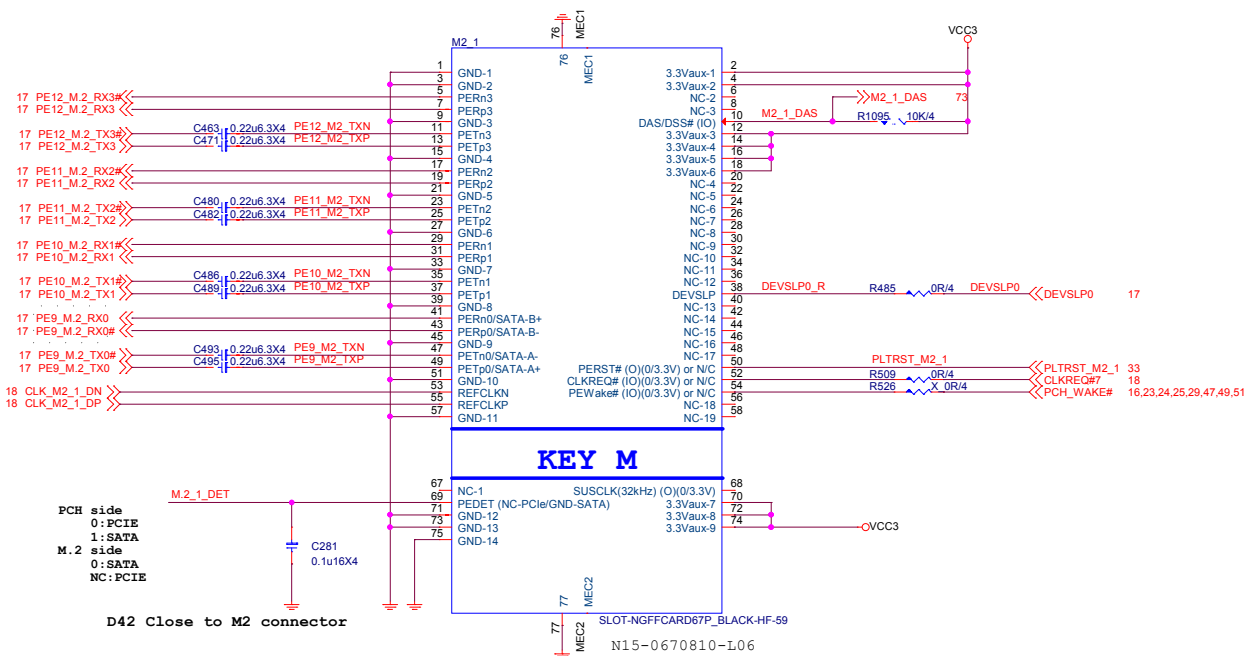








SATA 要反接  
PCH SATA#0

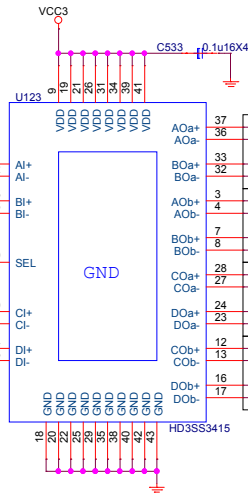




H:M2\_PCIE&SATA6  
L:M2\_SATA

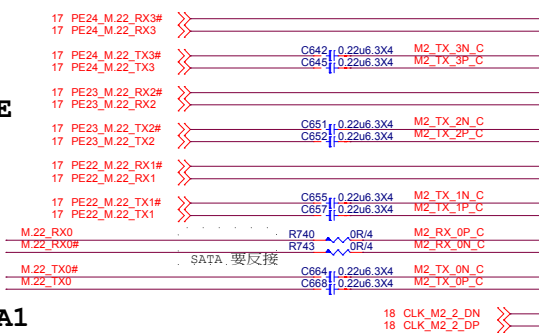
PCH SATA#1

SATA

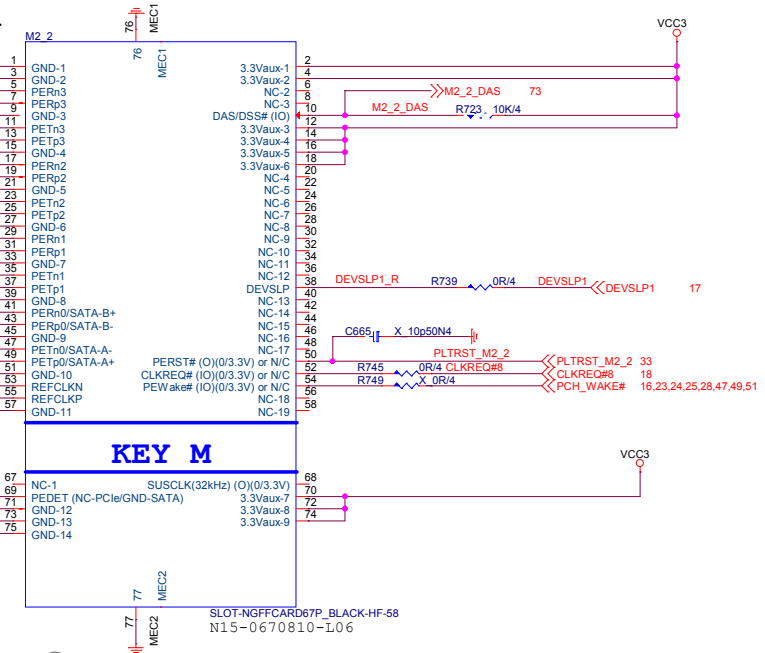


PCIE

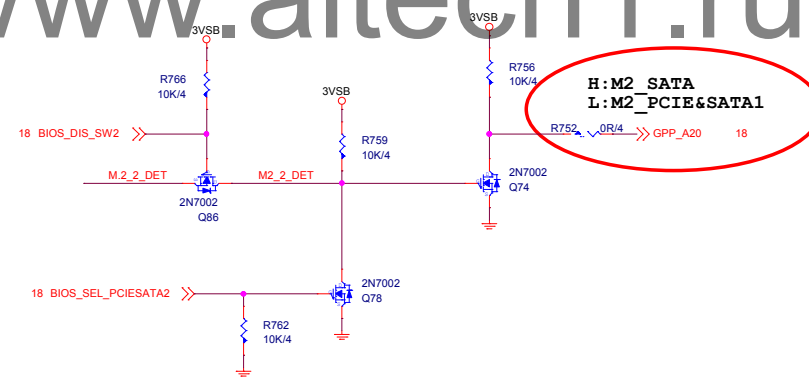
SATA1



2.5A

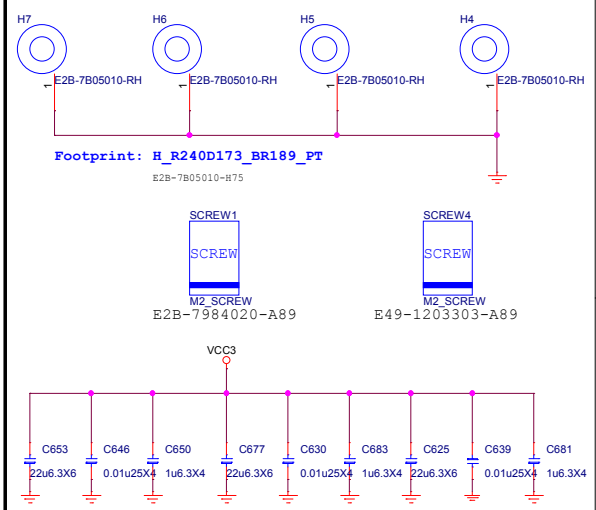



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BIOS\_MODE

BIOS_DIS_SW2	BIOS_SEL_PCIESATA2	Mode
0	1	M2-SATA
0	0	M2-PCIE
GPI (1)	GPI (1)	AUTO





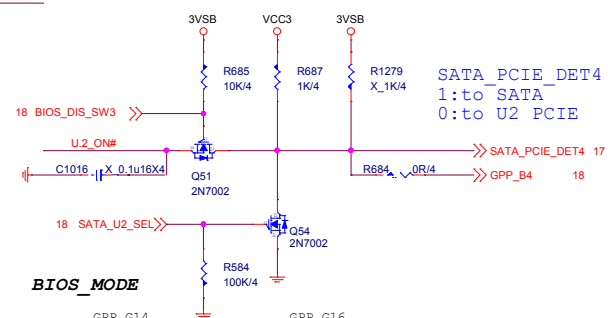
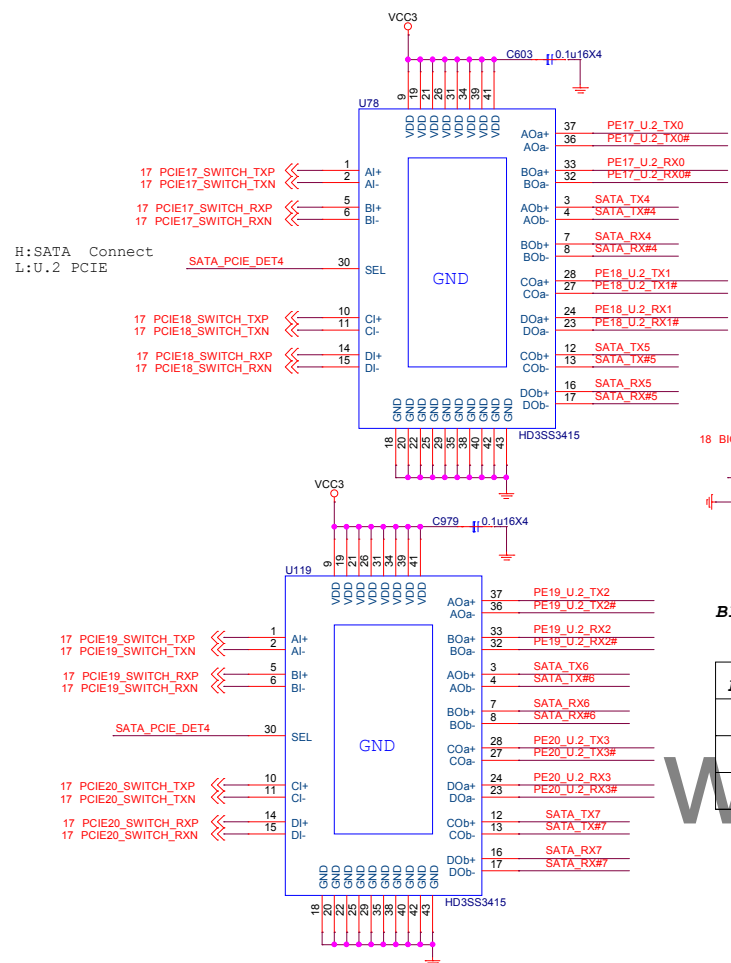
MICRO-STAR INT'L CO.,LTD

MS-7A95

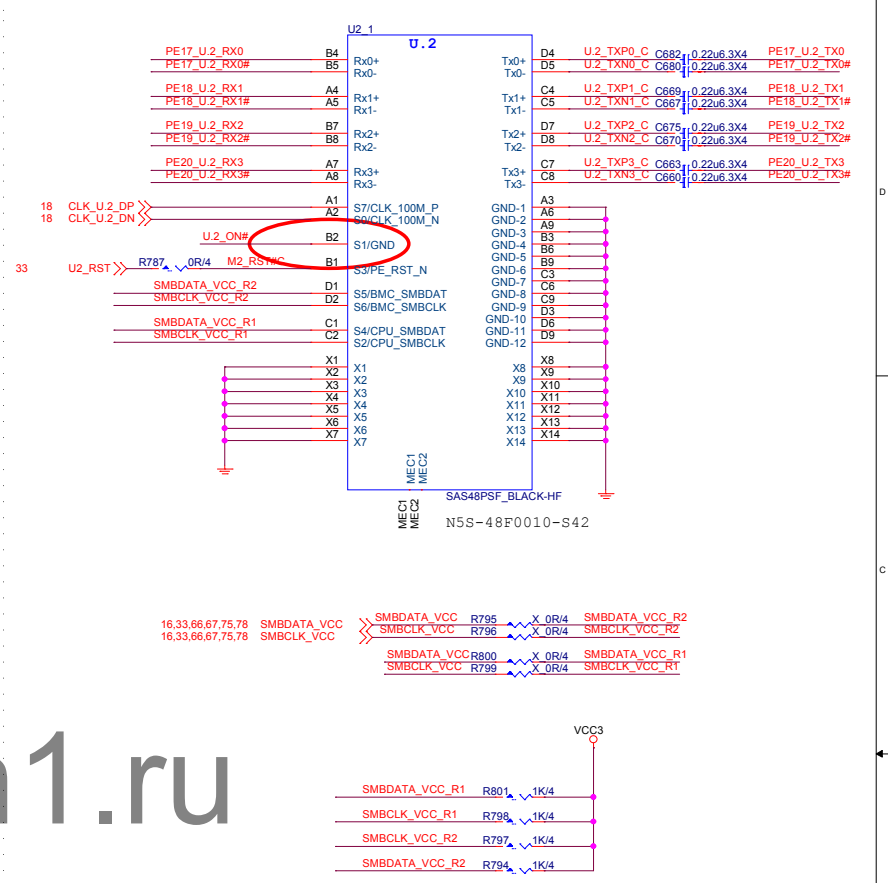
Size Custom Document Description Rev 1.0

Date: Monday, May 15, 2017

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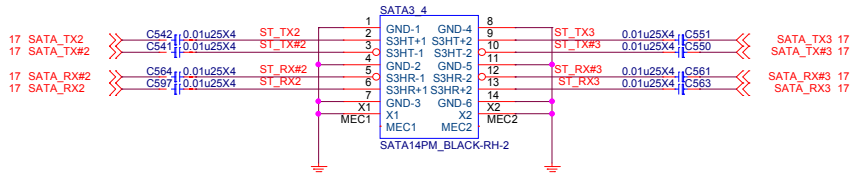
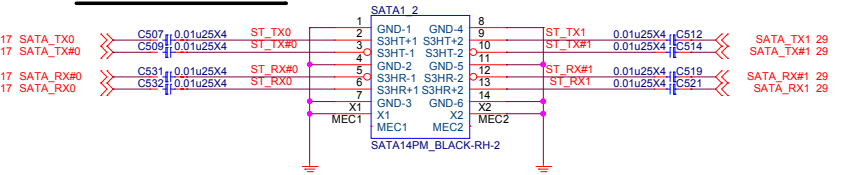
BIOS_DIS_SW3	SATA_U2_SEL	Mode
0	1	U2-PCIE
0	0	SATA5_6_7_8
GPI (1)	GPI (0)	AUTO



if M2\_1&M2\_2 use ,SATA1\_2 connect is no function.

### SATA 6G PORT 2.3 N5N-14M0201-L06

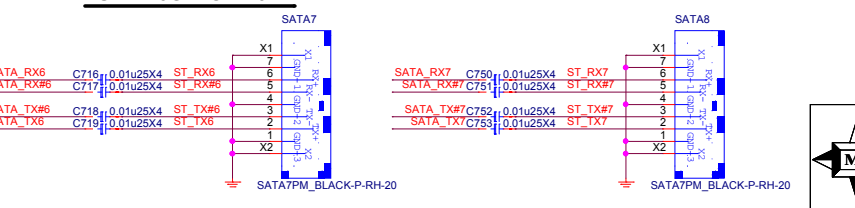
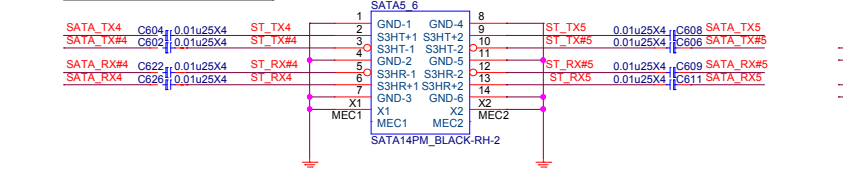
### SATA 6G PORT 0.1 N5N-14M0201-L06



if U\_2 use ,SATA5\_6、SATA7、SATA8 connect is no function.

### SATA 6G PORT 6.7 N5N-07M2441-H06

### SATA 6G PORT 4.5 N5N-14M0201-L06

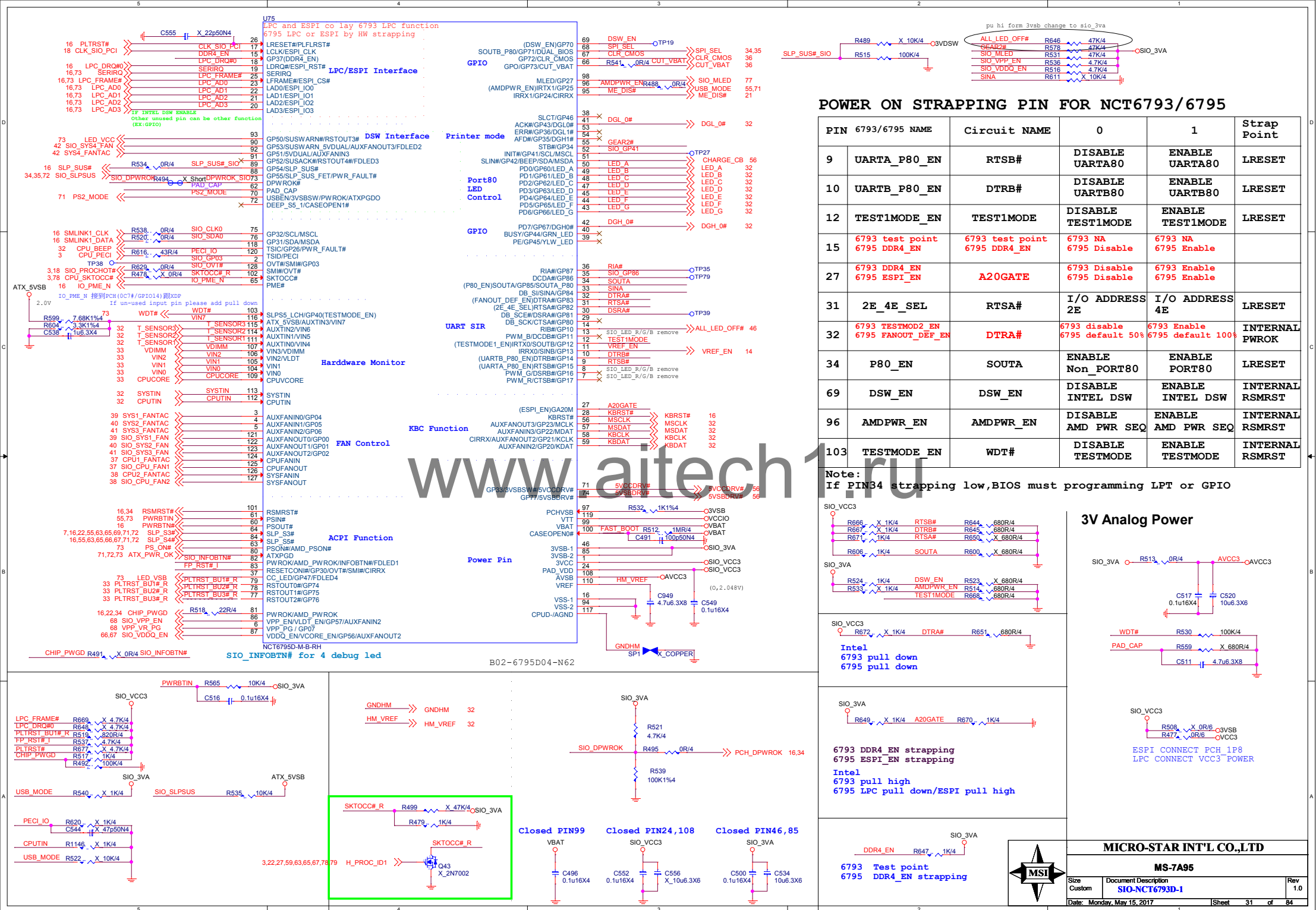


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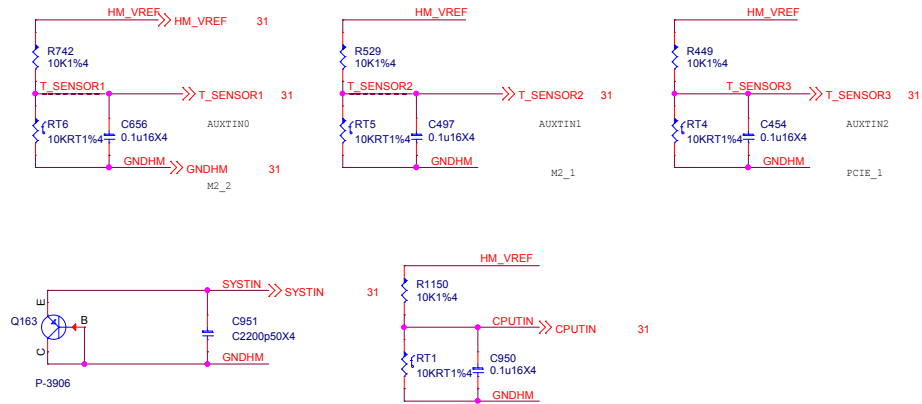
**MS-7A95**

Size: Custom    Document Description: **U2/SATA-Conn**    Rev: 1.0

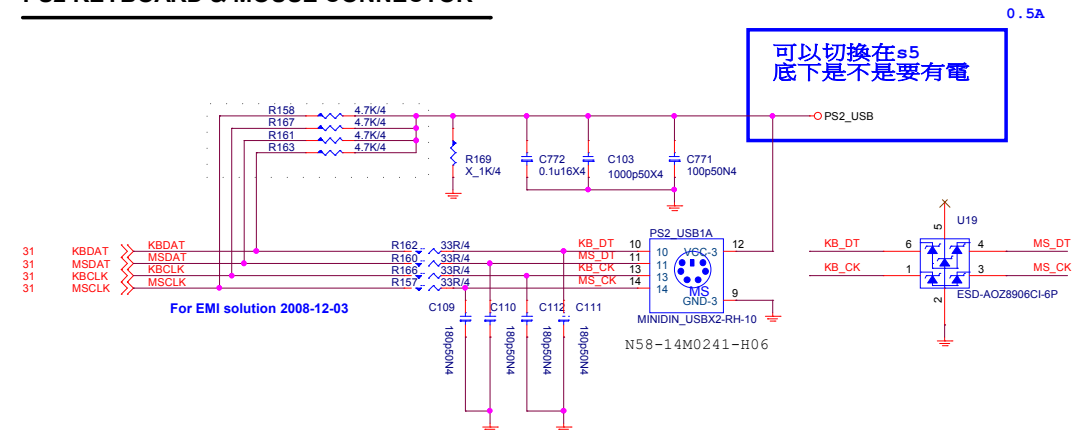
Date: Monday, May 15, 2017    Sheet: 30 of 84



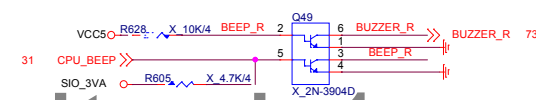
## THERMAL



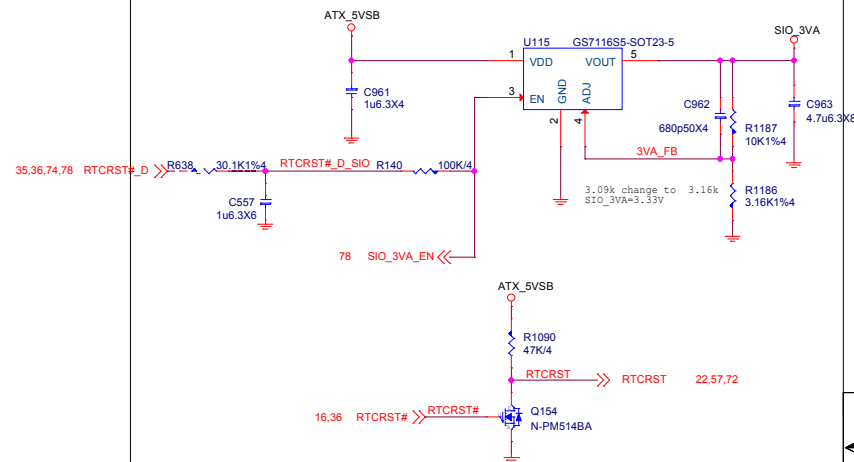
## PS2 KEYBOARD & MOUSE CONNECTOR



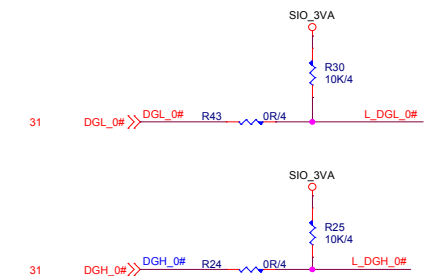
## COM Port for BIOS Debug



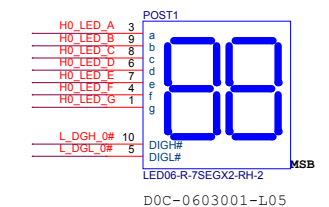
### SLP\_SUS Co-lay circuit



**DEBUG LED**



Debug LED OFF BIOS control

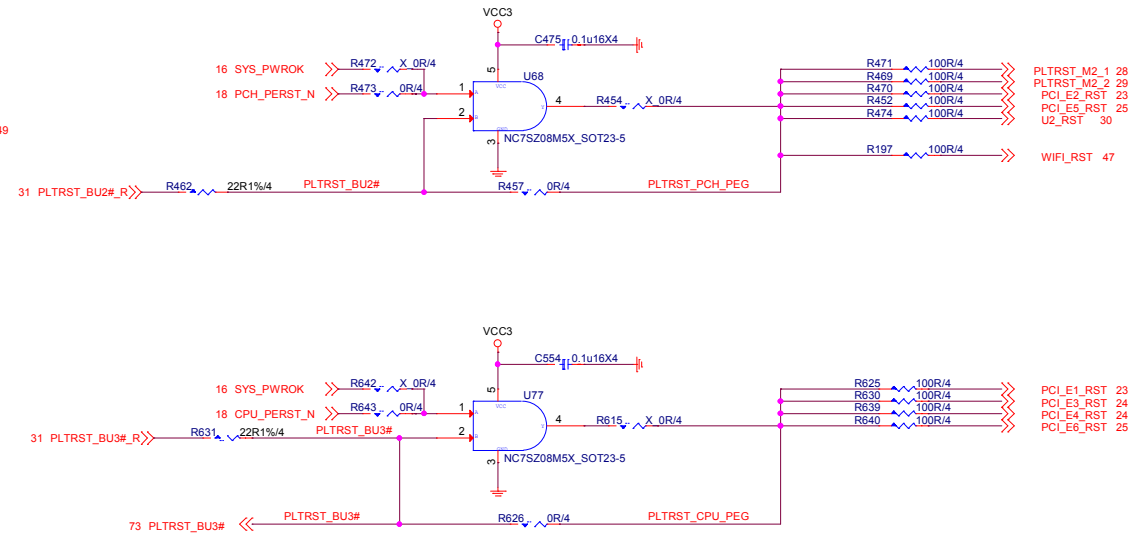
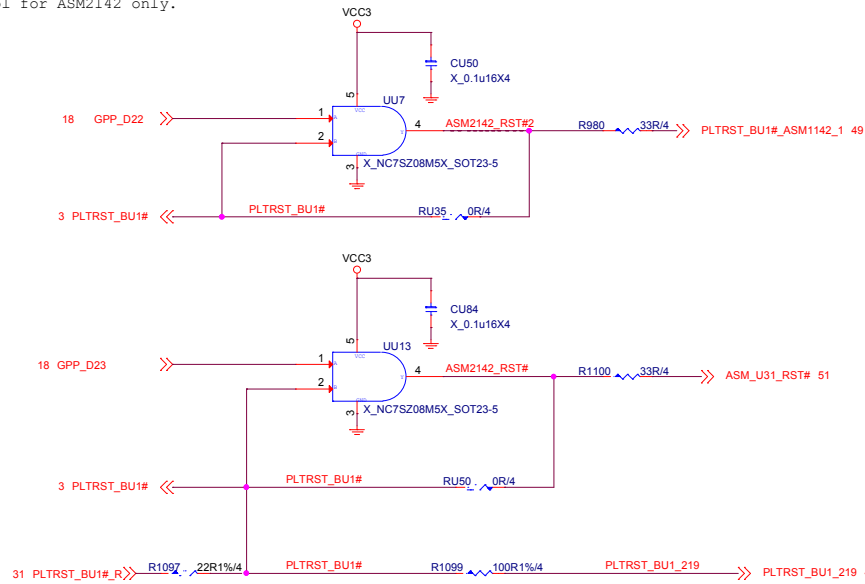


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MS-7A95

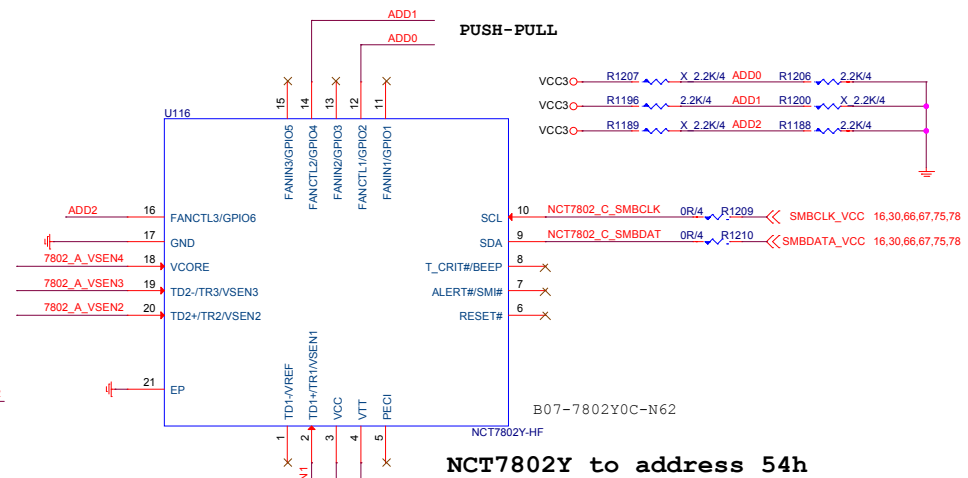
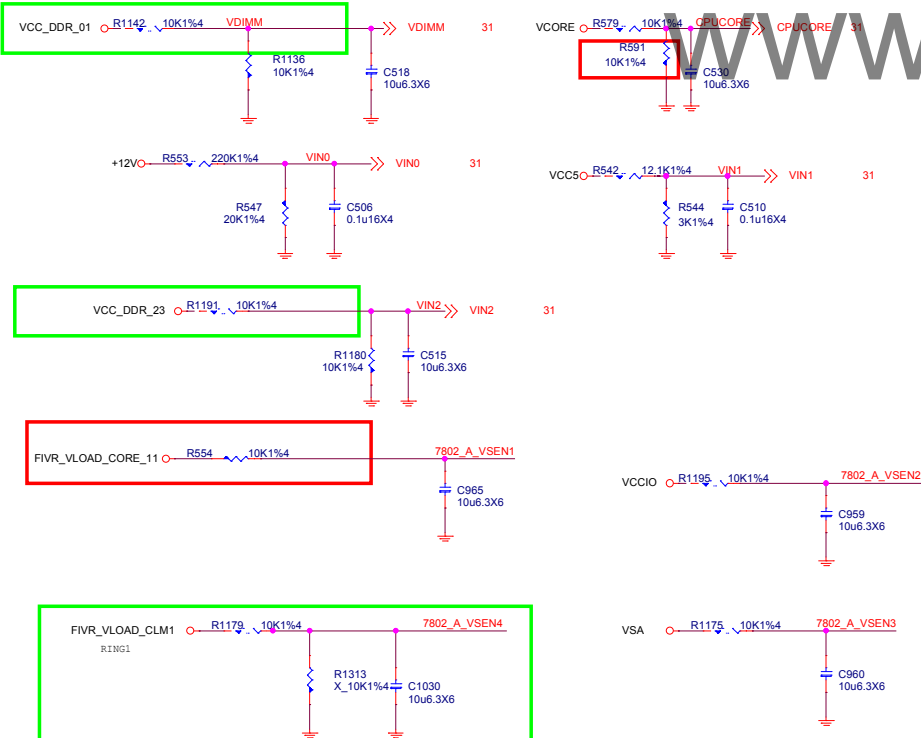
Size Custom	Document Description <b>SIO-NCT6793D-2</b>	Rev 1.0
Date: Monday, May 15, 2017		Sheet 32 of 84

Reset control for ASM2142 only.



## HW Monitor - Voltage

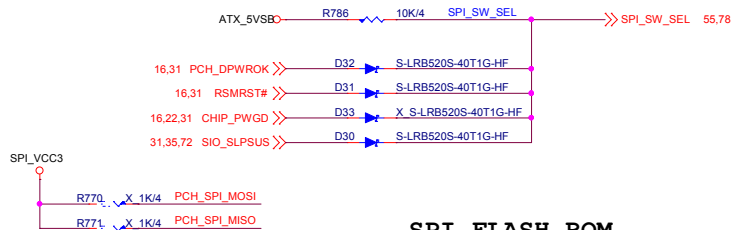
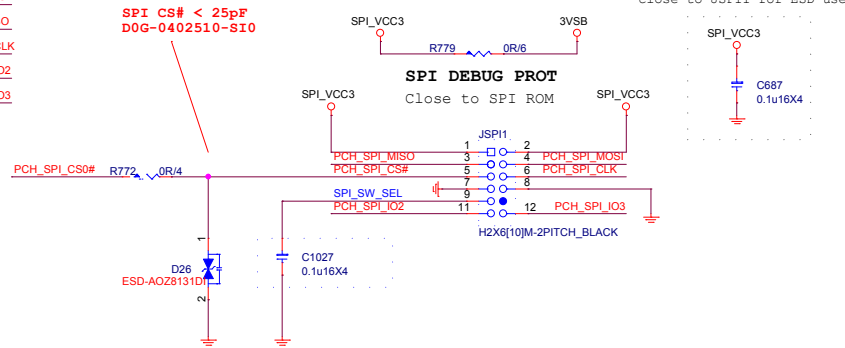
SIO HM Voltage voer 2V will not detect





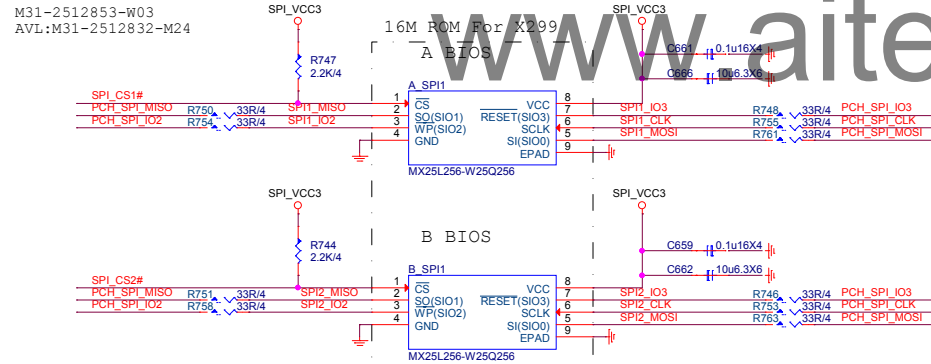
16.55 PCH\_SPI\_CS0# << PCH\_SPI\_CS0#  
 16.21.55 PCH\_SPI\_MOSI << PCH\_SPI\_MOSI  
 16.21.55 PCH\_SPI\_MISO << PCH\_SPI\_MISO  
 16.55 PCH\_SPI\_CLK << PCH\_SPI\_CLK  
 16.21 PCH\_SPI\_IO2 << PCH\_SPI\_IO2  
 16.21 PCH\_SPI\_IO3 << PCH\_SPI\_IO3

Part Number: N31-2061341-H06



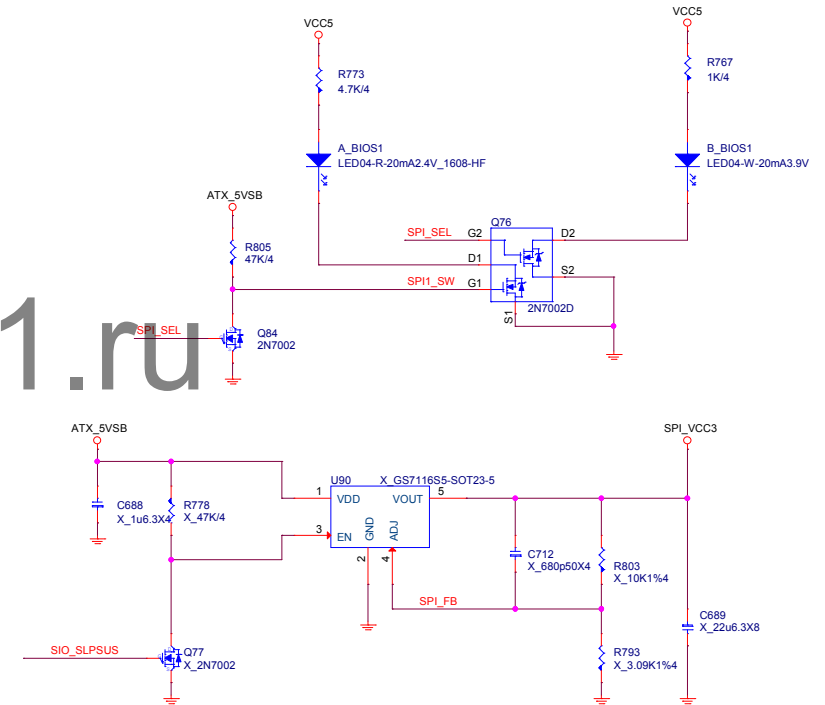
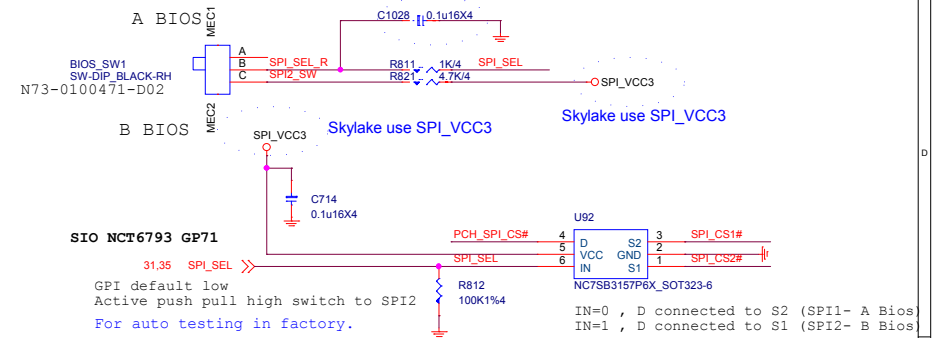
### SPI FLASH ROM

Place close to SB.



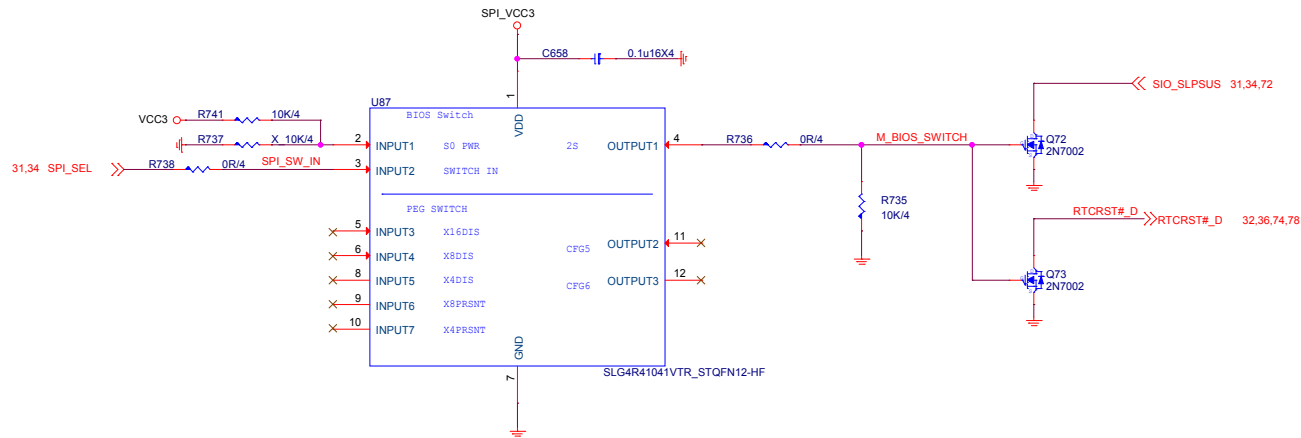
\*SPI\_CLK & SPI\_MOSI must be length matched to within 500mils. < 6 inch  
 \*SPI\_CLK & SPI\_CS0# must be length matched to within 500mils.

HW MODE



MICRO-STAR INT'L CO.,LTD			
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Size Custom	Document Description Dual BIOS		Rev 1.0
Date: Monday, May 15, 2017	Sheet	34	of 84

# Skylake/Kabylake Path Circuit For Dual Bios



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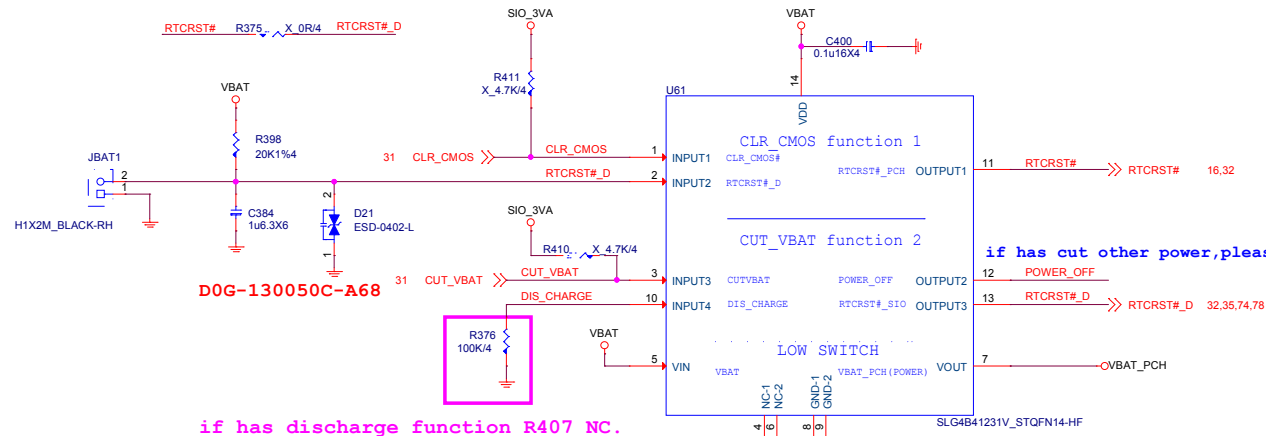
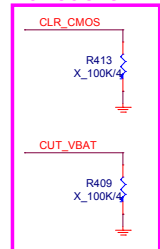


MICRO-STAR INT'L CO.,LTD

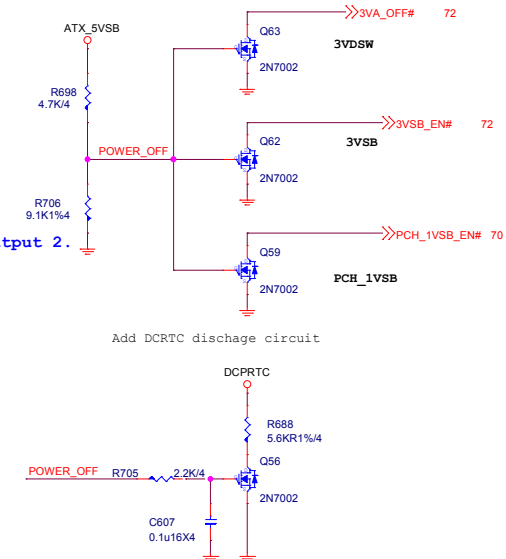
MS-7A95

Size Custom	Document Description Dual bios control-Silego	Rev 1.0
Date: Monday, May 15, 2017	Sheet 35 of 84	

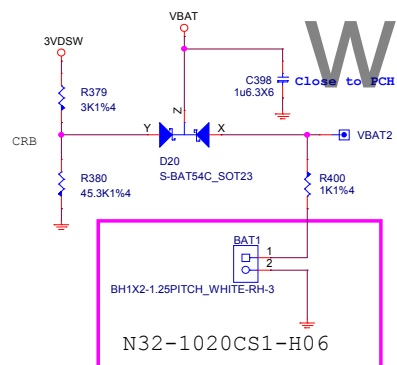
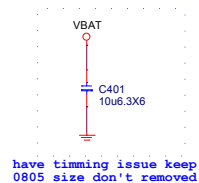
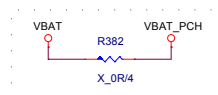
20160629



if has discharge function R407 NC.



## VBAT



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# TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

From SIO

31 SIO\_CPU\_FAN1

18 CPUFAN1\_MODE

FIX MODE unstuff

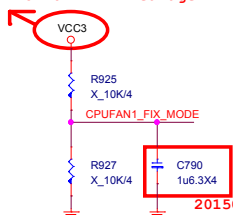
PWM Mode : VOUT voltage follows VIN voltage  
DC Mode : VOUT voltage is regulated to 3.8\*DCIN voltage.

NCT3947S-A\_SOP8-HF-1

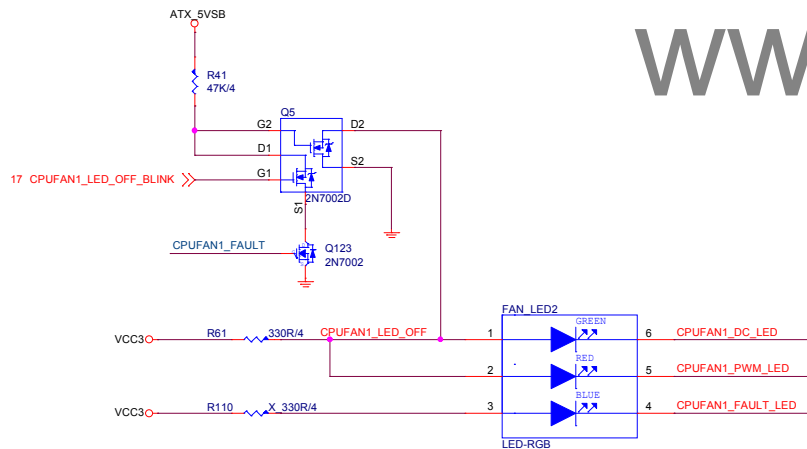
GPIO Control	
	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI (Floating)
Internall pull up 1.65V	

Default

Avoid NCT3947S MODE PIN Leakage



Resever For FIX DC or PWM MODE USE By PM SPEC



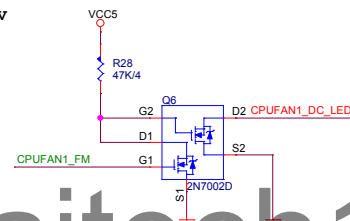
Forward Current 20mA  
Pulse Forward Current 40-60mA

RGB  
D0C-040S400-H91

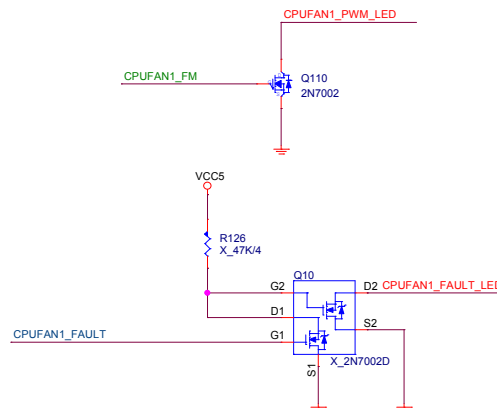
DC\_FAN\_LED (綠)  
PWM\_FAN\_LED (藍)  
FAN\_OCP\_LED (紅)

CPUFAN\_PWR  
>40mil

C22,C23,C263 close to FAN Connector



CHECK NCT3947S Sink Current

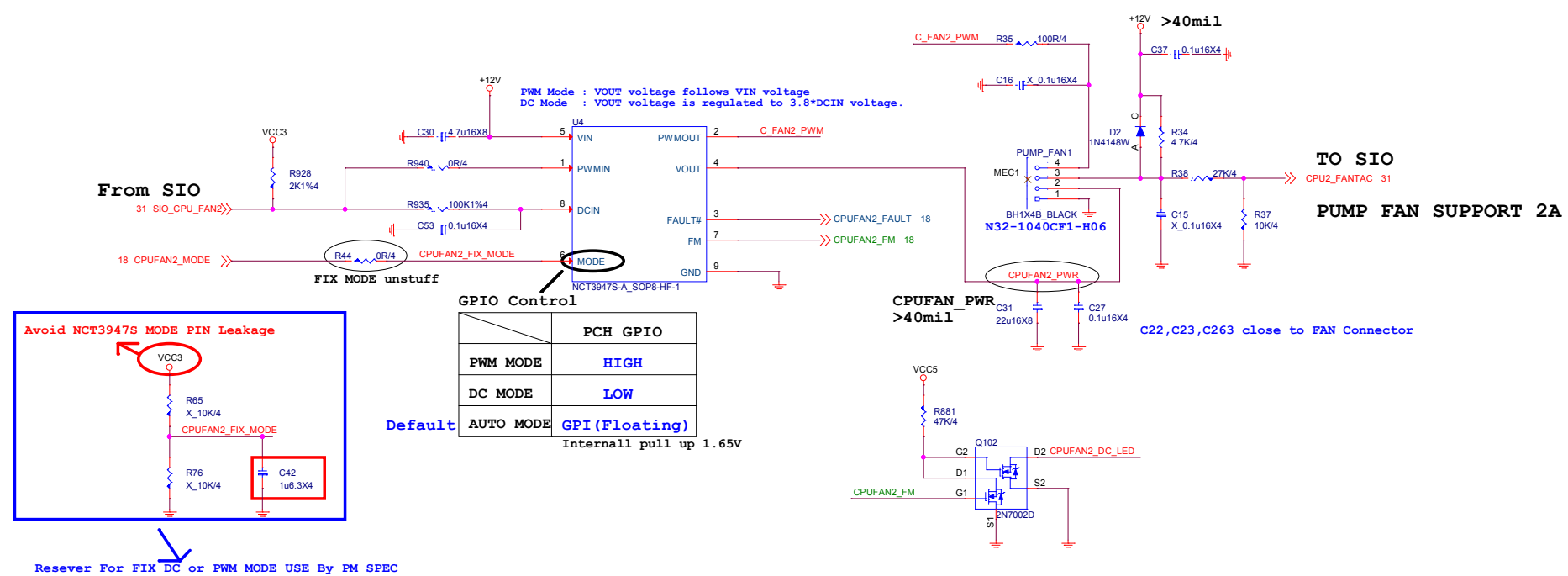


MICRO-STAR INT'L CO.,LTD

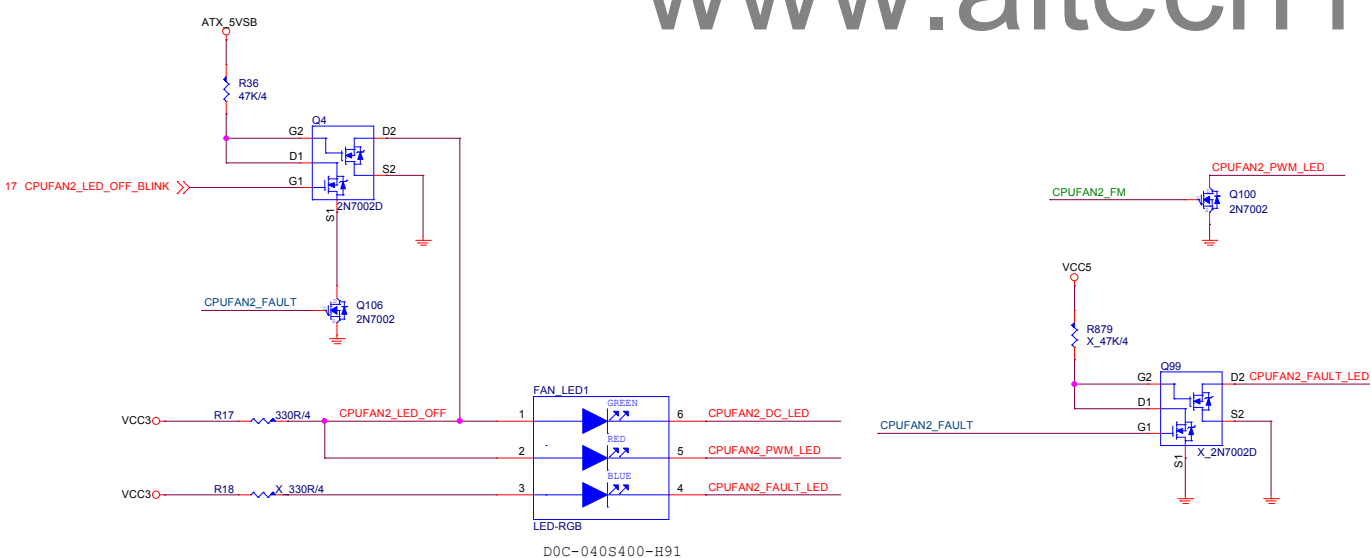
MS-7A95

Size Custom	Document Description CPU FAN1	Rev 1.0
Date: Monday, May 15, 2017	Sheet 37 of 84	

# TYPE J : 4 PIN PUMP FAN USE NCT3947S USE PCH GPIO



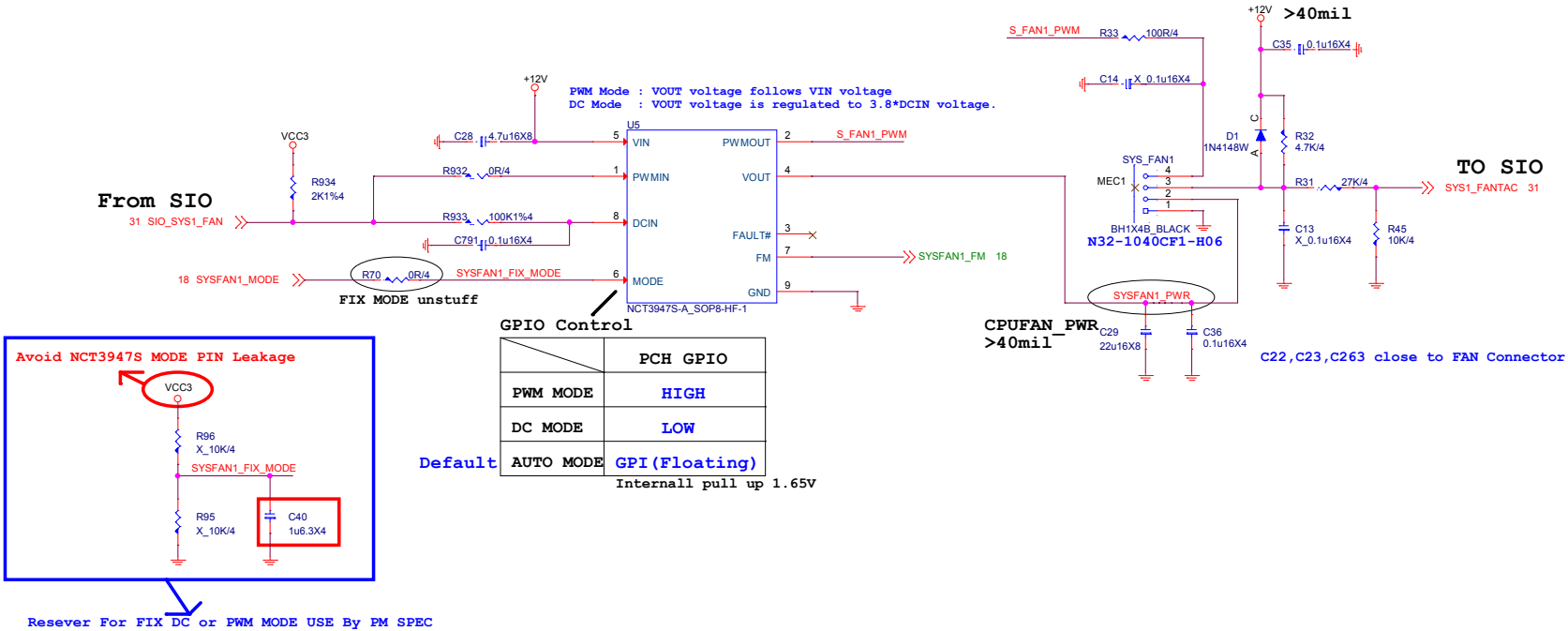
www.aitech1.ru



CHECK NCT3947S Sink Current

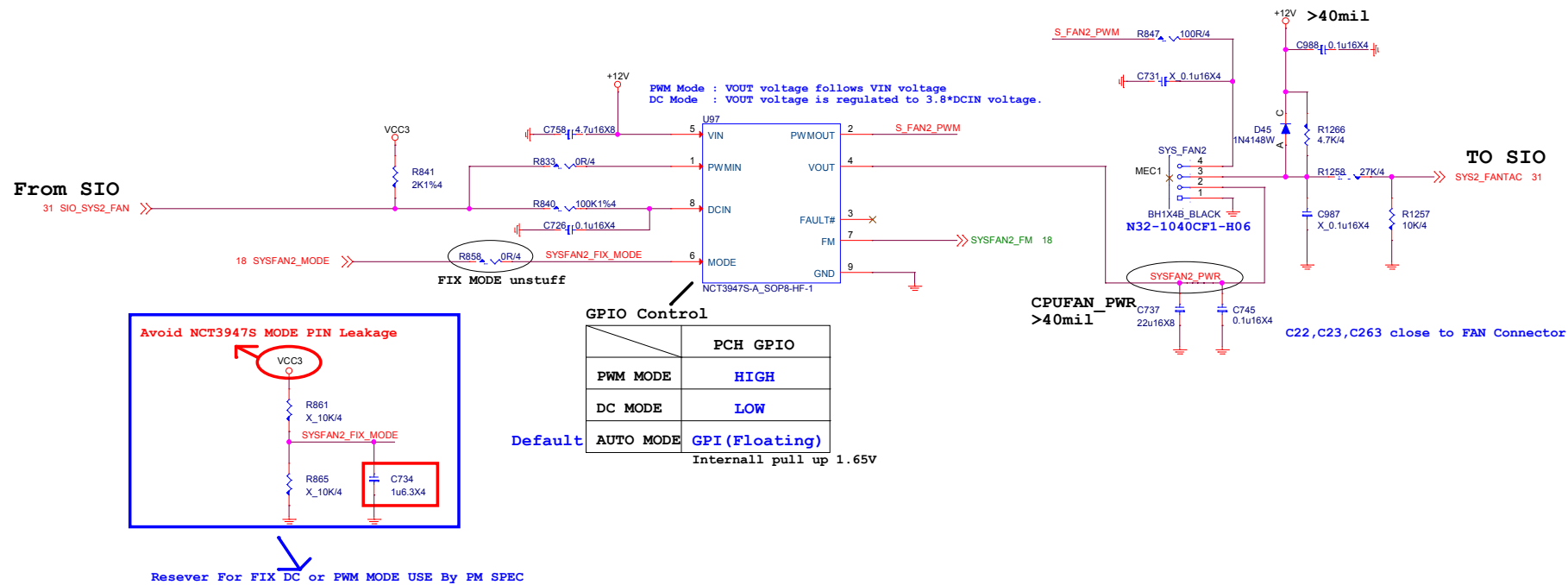


TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



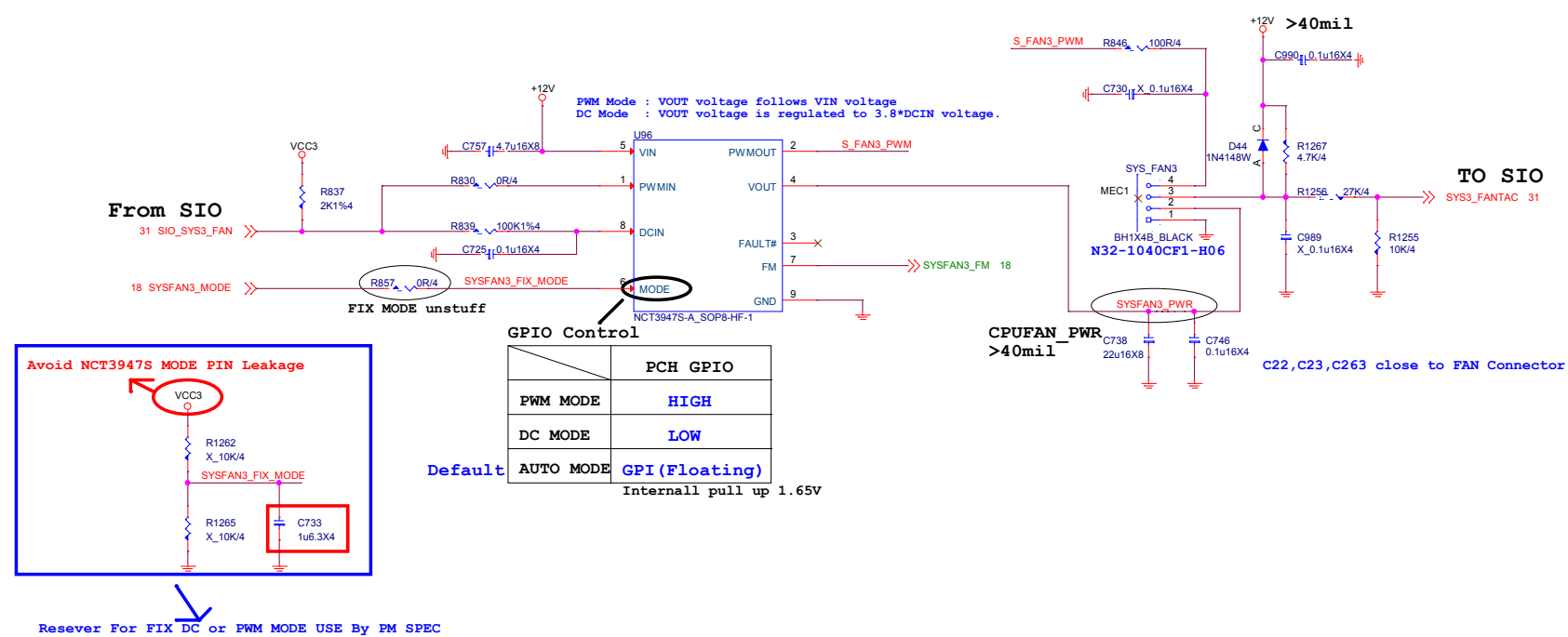
www.aitech1.ru

TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



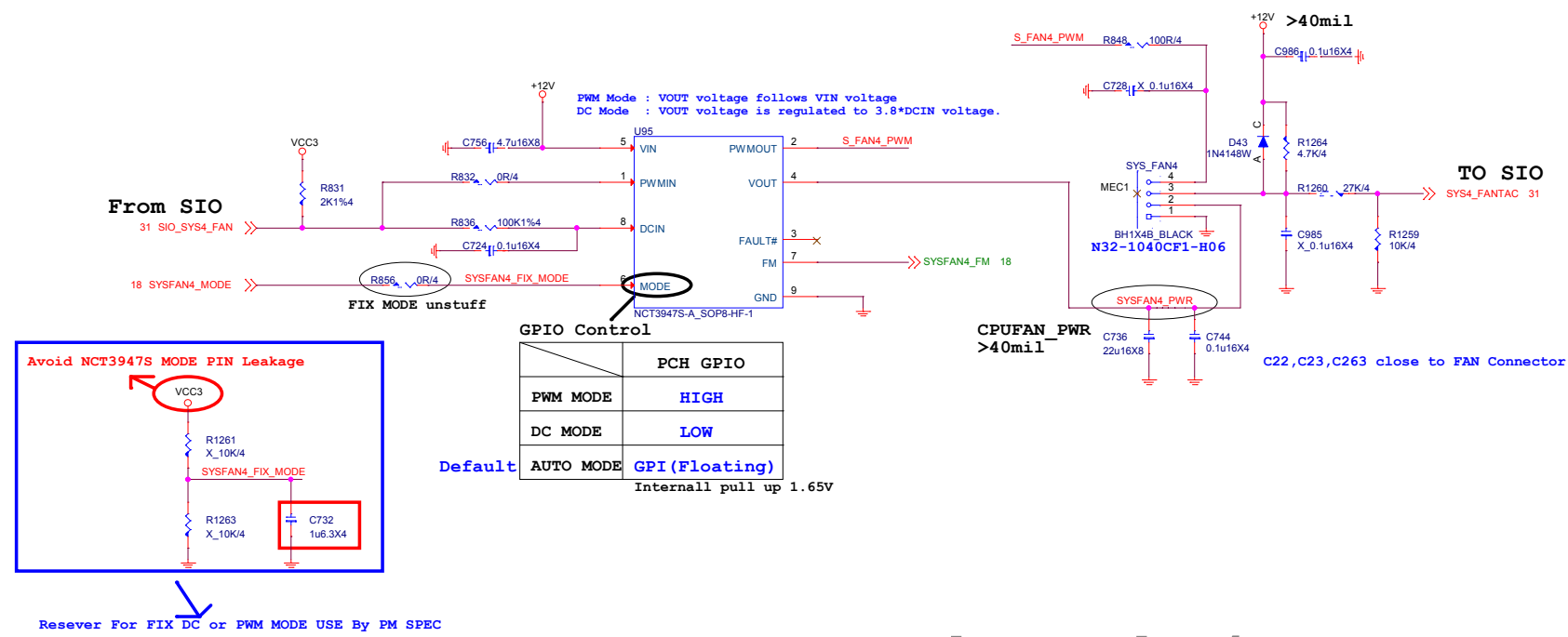
[www.aitech1.ru](http://www.aitech1.ru)

# TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



www.aitech1.ru

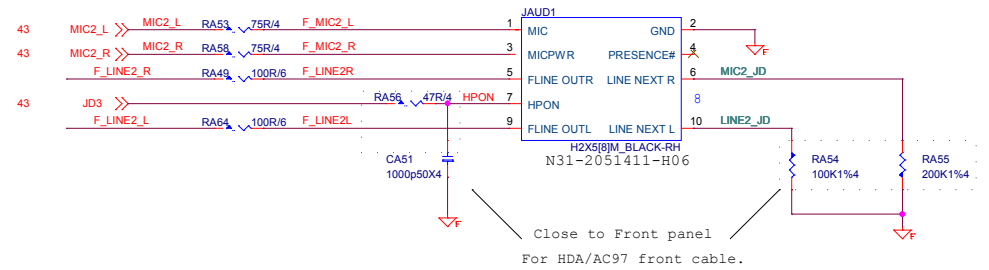
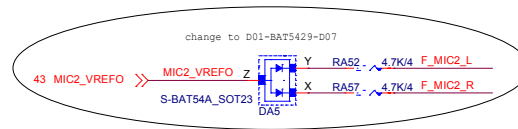
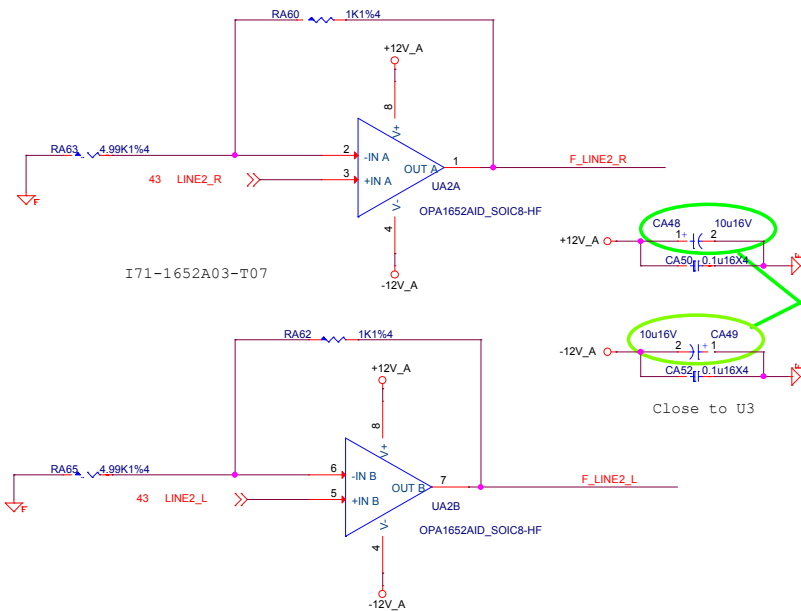
# TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



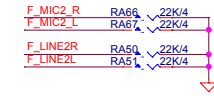
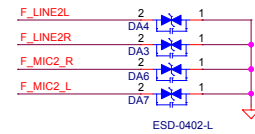
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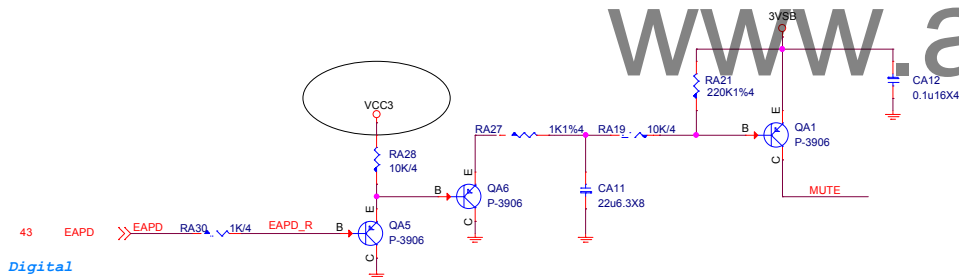


Close to Jack  
**ESD protect**  
 D0G-2950500-SI0  
 D0G-3010510-I05

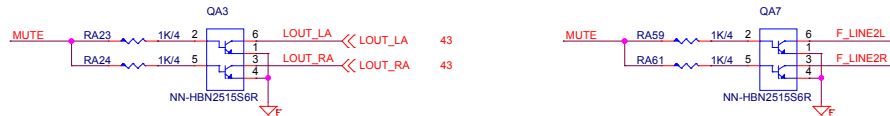


# **Rear Line OUT De-POP circuit** (De-pop circuit for Rear Line out & Front Headphone out)

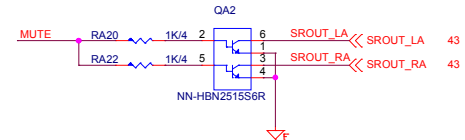
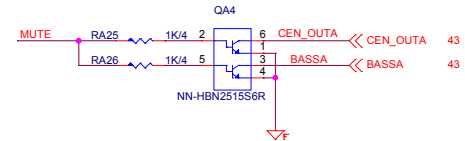
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Analogue



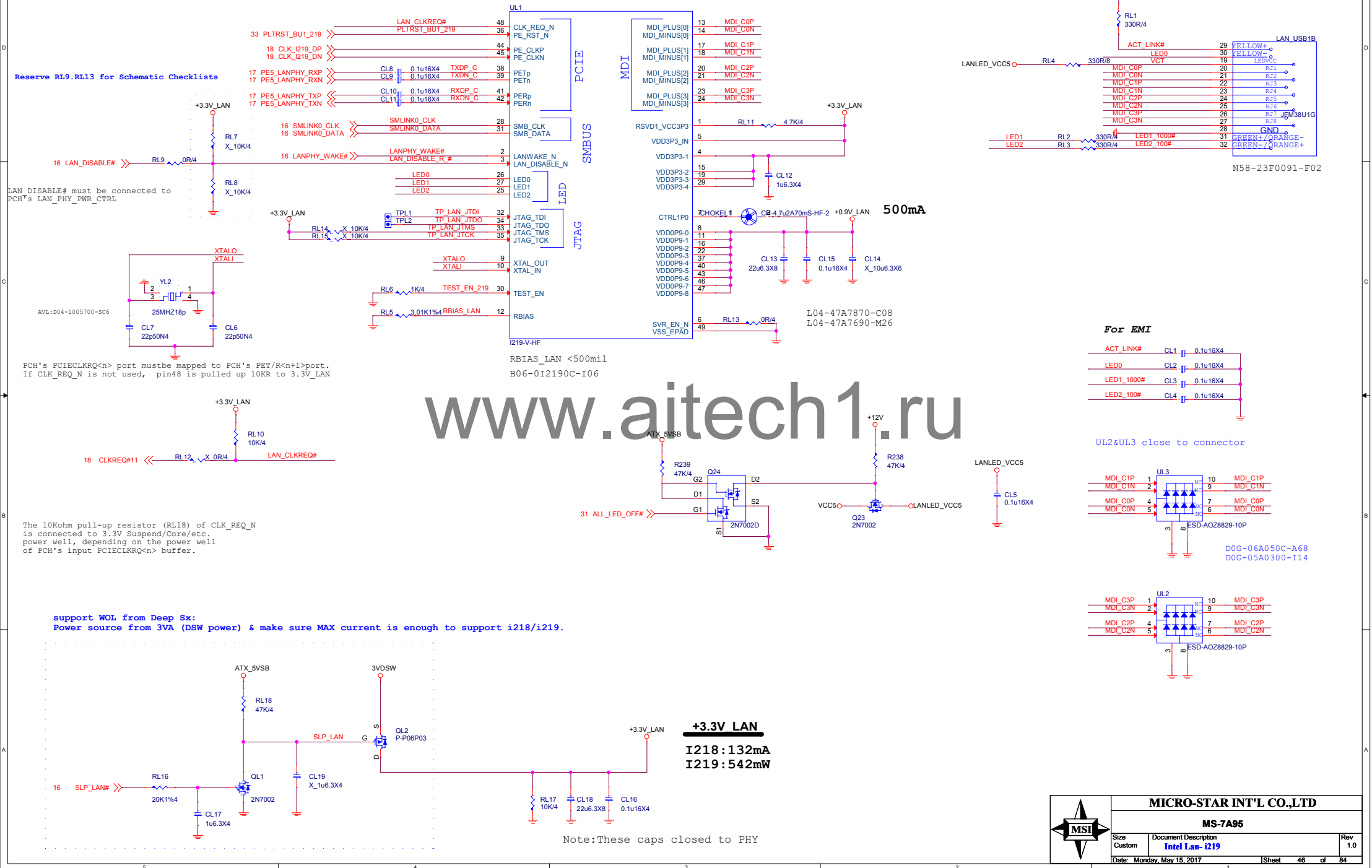
(add de-pop circuit by PM spec or customer request,  
 NOTE: add de-pop circuit need to change CA6, CA7, CA12, CA13, CA23, CA24 to TVS)



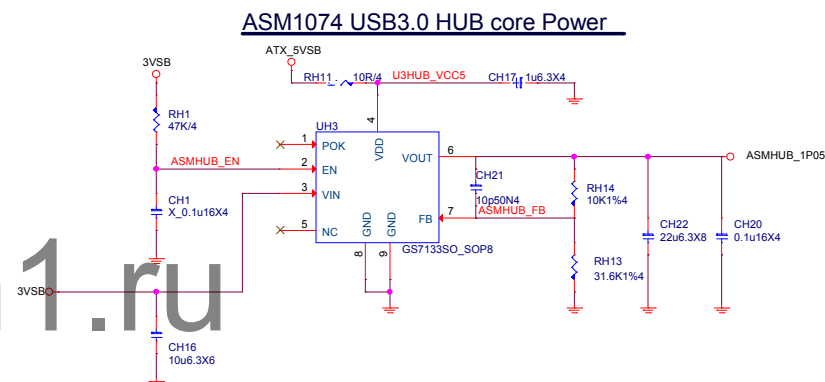
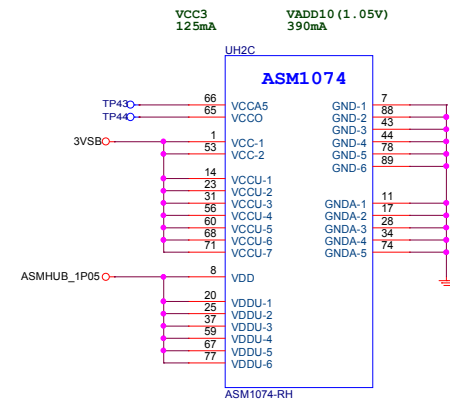
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			MICRO-STAR INT'L CO.,LTD		
			MS-7A95		
Size	Document Description			Rev	
Custom	AUDIO-ACL1220-3			1.0	
Date: Monday, May 15, 2017			Sheet	45	of 84

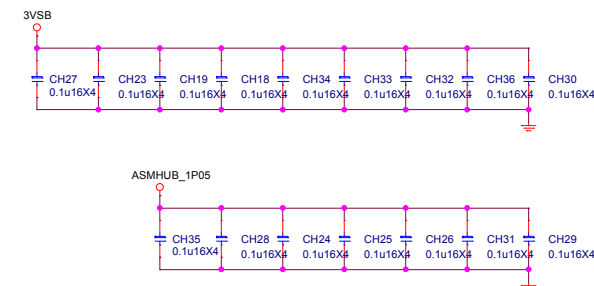
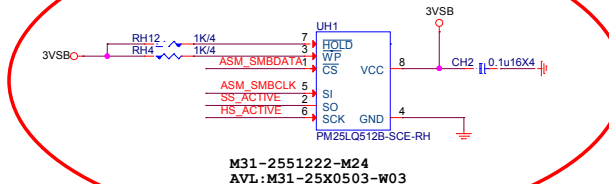
# Intel I219V / I218V PHY







GRN LED2 (CLK_SEL1)	GRN LED1 (CLK_SEL0)	
0	0	25MHz
1	0	30MHz
1	1	20MHz

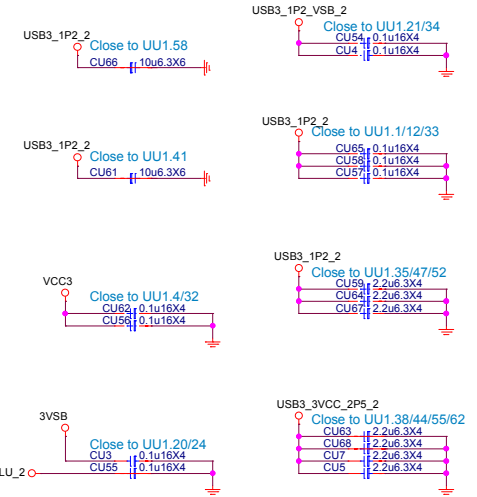
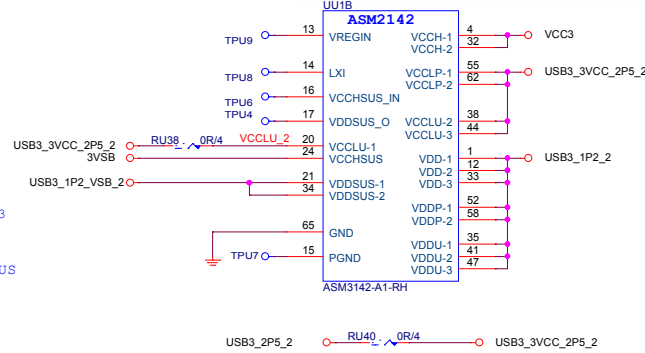
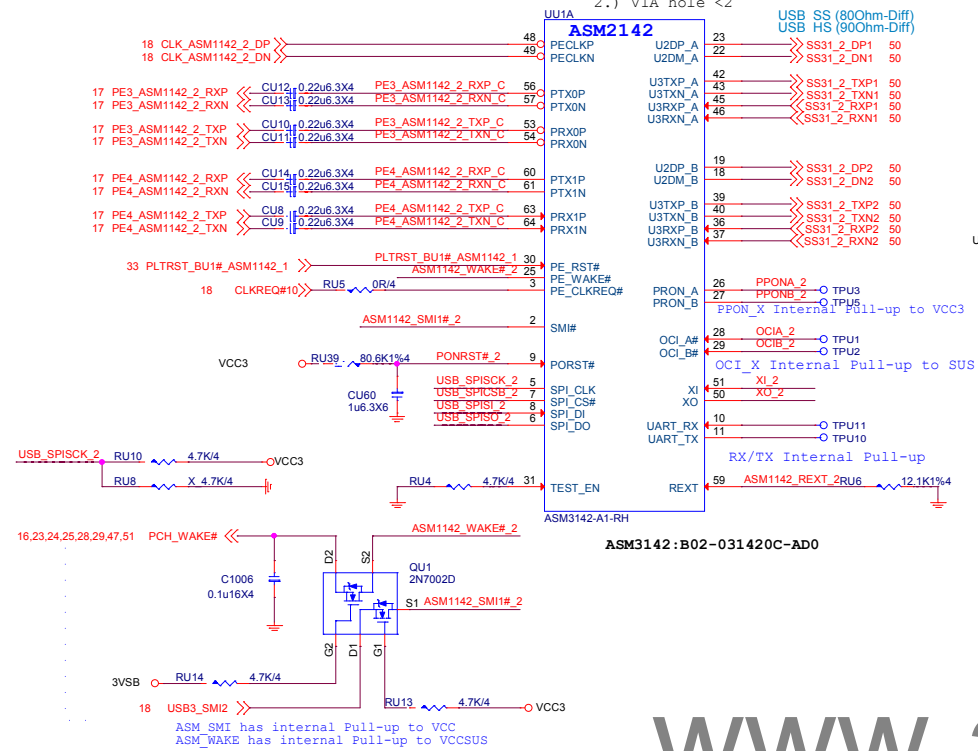




- Layout Guide:
- 1.) USB3.1 to Connector Total Length < 1.5"
  - 2.) VIA hole < 2

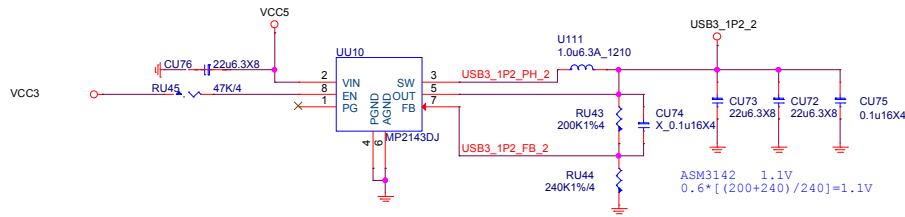
#### Power Consumption

	3.3V	1.2V(1.05V)	3.3VSUS	1.05VSUS(1.2VSUS)	2.5V	Total Power
ASM1142	245mA	634mA	1mA	1mA	NA	1573.8(mW)
ASM2142	300mA	800mA	100mA	50mA	300mA	TDP
ASM3142	TBD	TBD	TBD	TBD	TBD	TBD

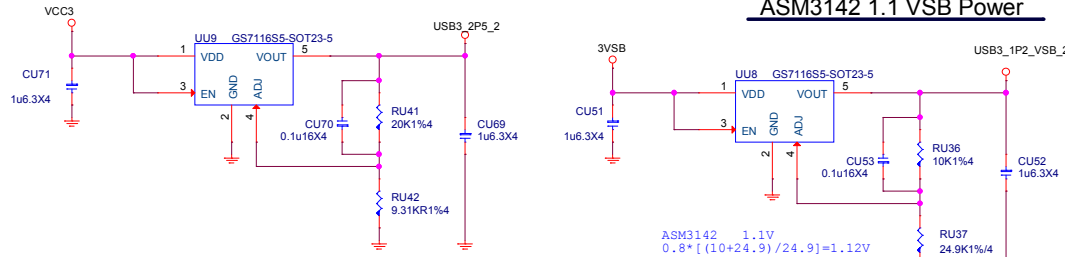


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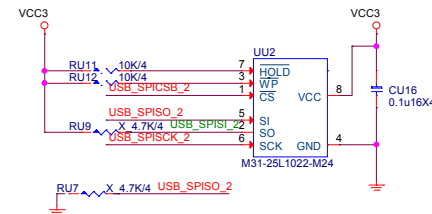
#### ASM3142 1.1 VCC Power



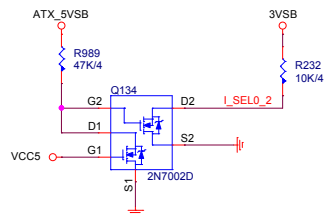
#### ASM3142 1.1 VSB Power



#### EEPROM



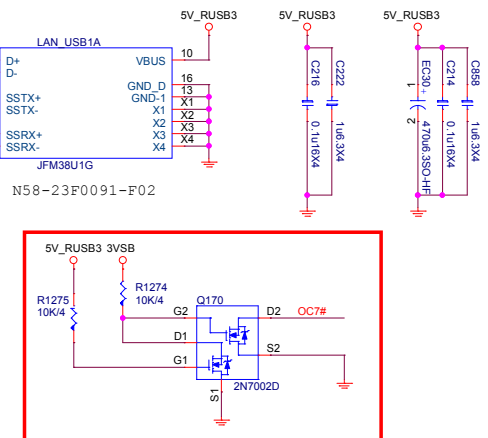
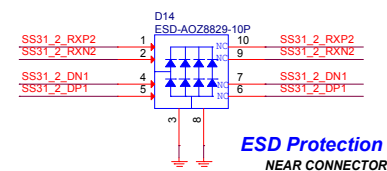
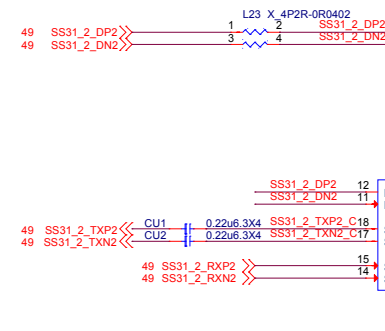
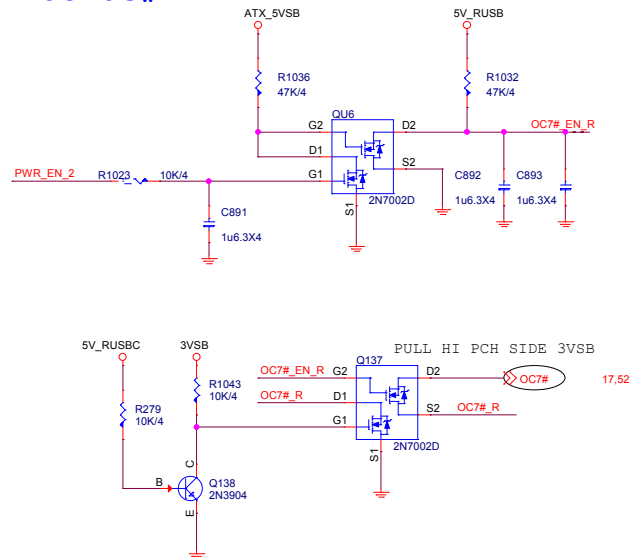
## Current Mode



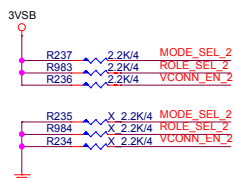
0	X	Default for 900mA
1	0	1.5A @5V
1	1	3A @5V

1.5A under S3 mode  
3A under S0 mode

## VBUS OC#



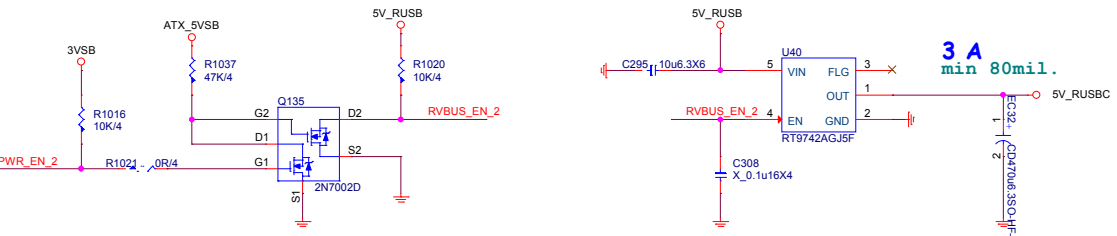
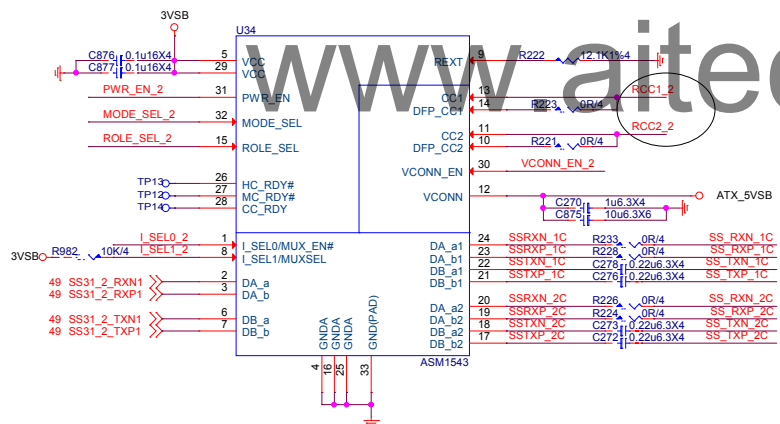
## USB Type-C MUX with Configuration Channel (CC)



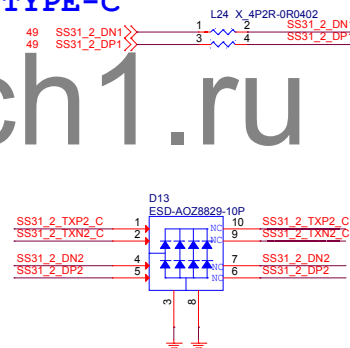
MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFP role (default)
0	UFP role

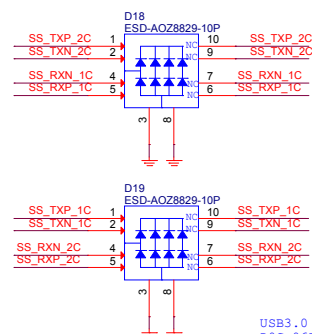
VCONN_EN	
1	enable
0	disable



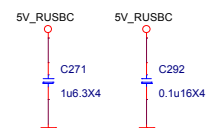
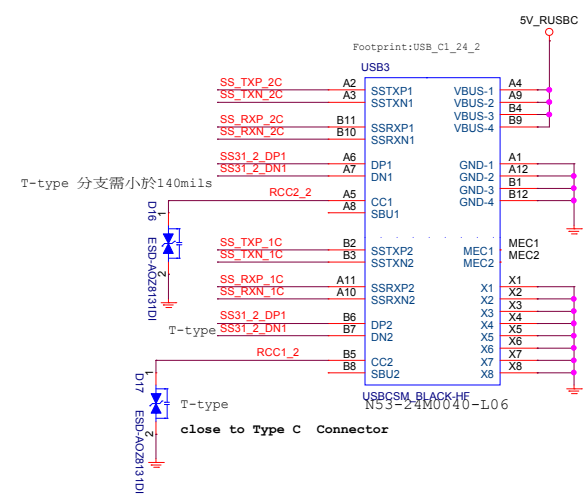
## TYPE-C



ESD Protection  
NEAR CONNECTOR



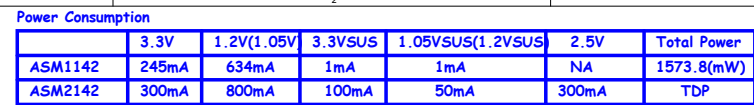
USB3.0  
DQG-06A050C-A68 Main  
DQG-05A0300-I14 AVL  
DQG-45B031C-005 AVL



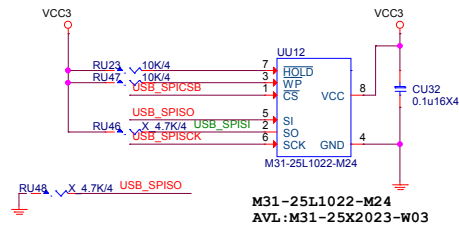
MICRO-STAR INT'L CO.,LTD			
MS-7A95			
Size	Document Description	Rev	
Custom	USB TYPEC-A-2	1.0	
Date:	Monday, May 15, 2017	Sheet	50 of 84

Layout Guide:

- 1.) USB3.1 to Connector Total Length < 1.5"
- 2.) VIA hole < 2



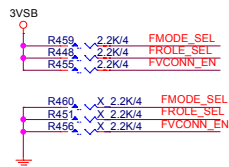
## EEPROM

**MS-7A95**

Size Custom	Document Description <b>51.ASM2142AE FRONT-USB31-2</b>	Rev 1.0
Date: Tuesday, May 16, 2017	Sheet 51 of 84	

# USB 3.1-Type-C

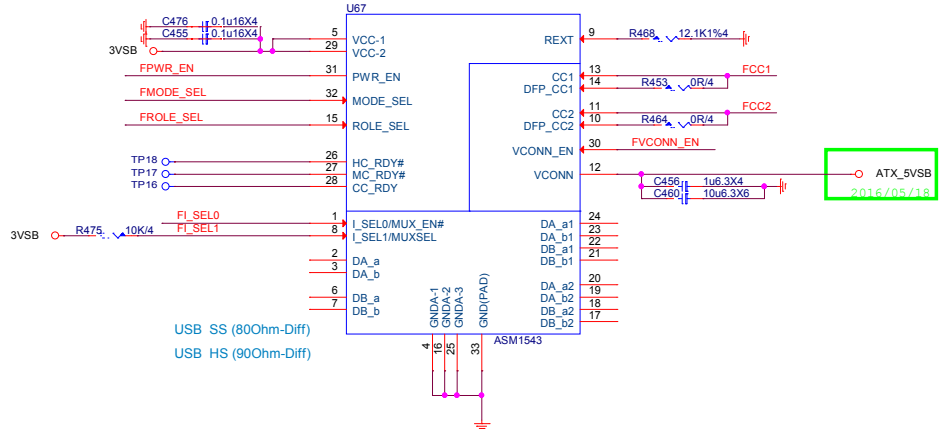
## USB Type-C MUX with Configuration Channel (CC)



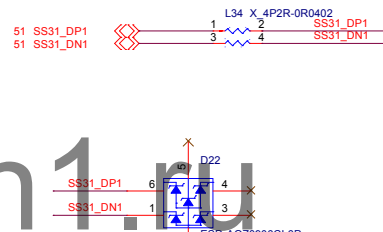
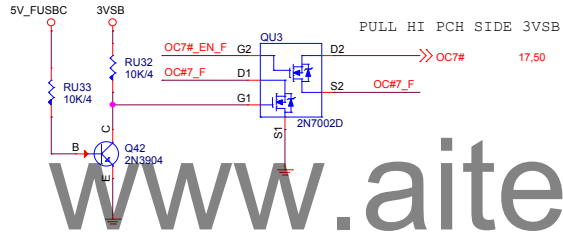
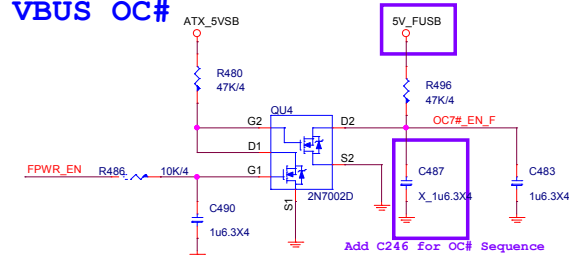
MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFP role (default)
0	UFP role

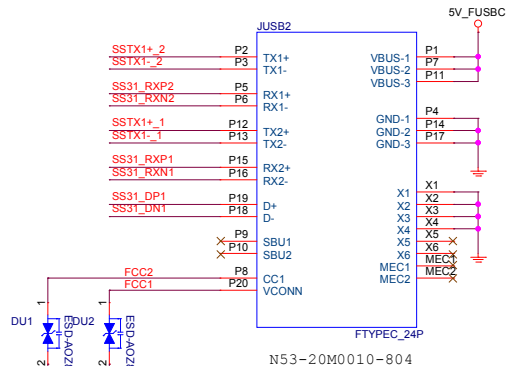
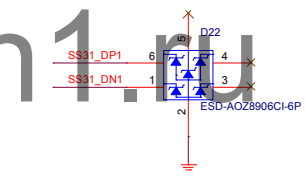
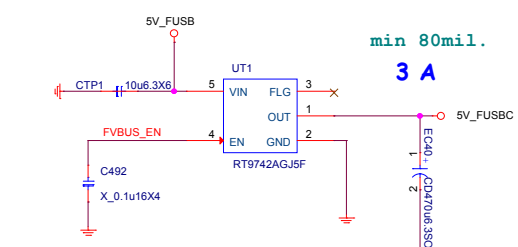
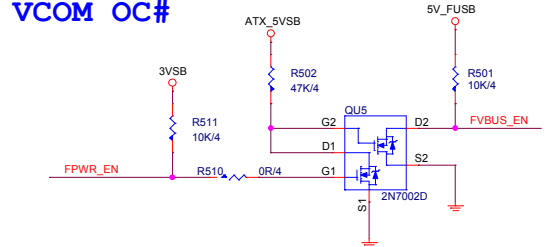
VCONN_EN	
1	enable
0	disable



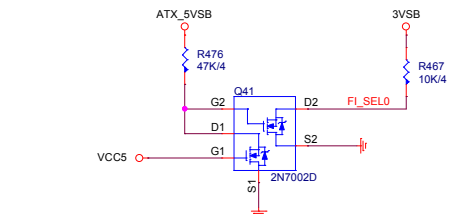
### VBUS OC#



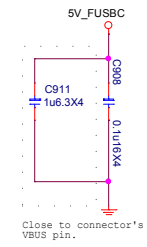
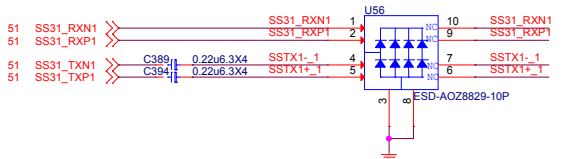
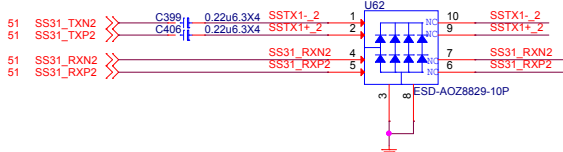
### VCOM OC#



### Current Mode



I_SEL0 : I_SEL1	
X 0	Default for 900mA
0 1	1.5A @5V
1 1	3A @5V



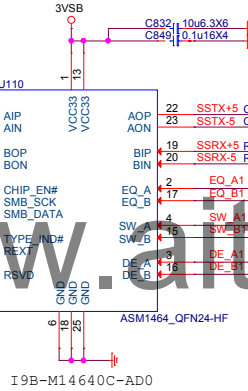
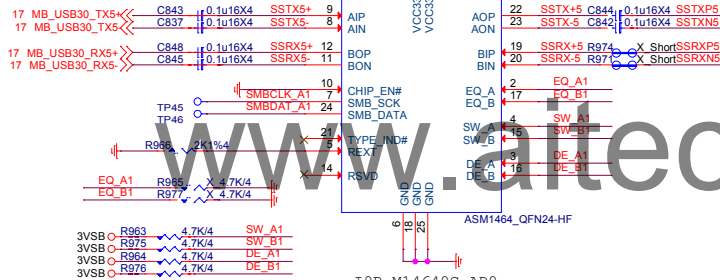
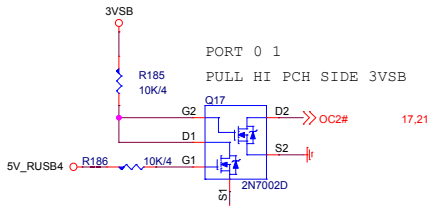
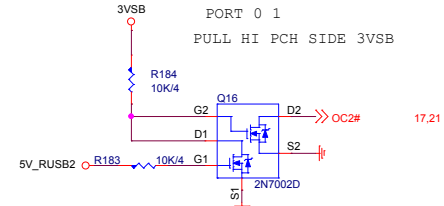
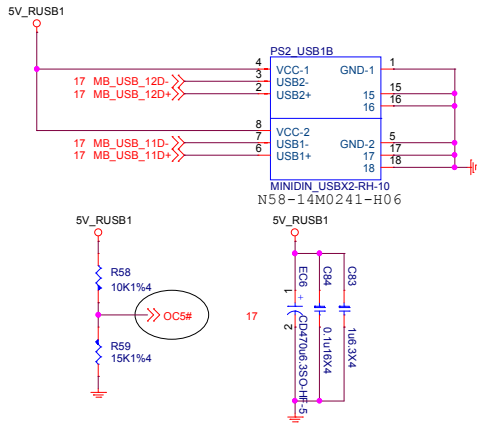
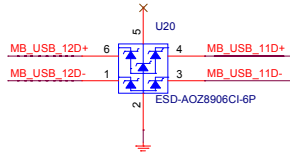
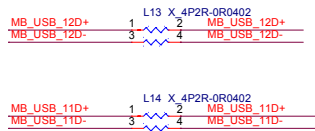
**MICRO-STAR INT'L CO.,LTD**

**MS-7A95**

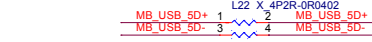
Size Custom Document Description **USB FRONT TYPE-C** Rev 1.0

Date: Monday, May 15, 2017 Sheet 52 of 84

## PS2\_USB1



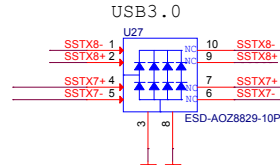
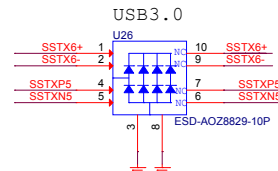
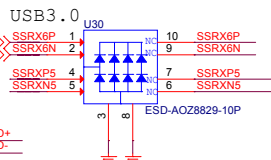
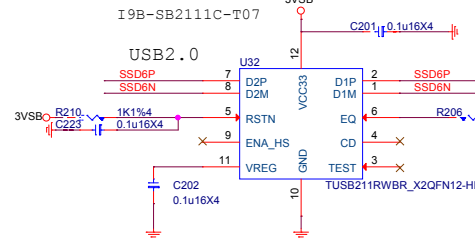
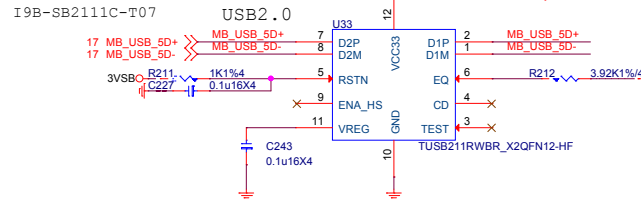
USB2.0



USB2.0

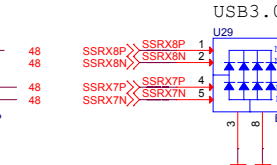


USB2.0

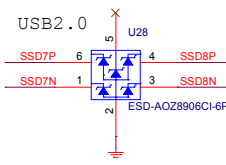
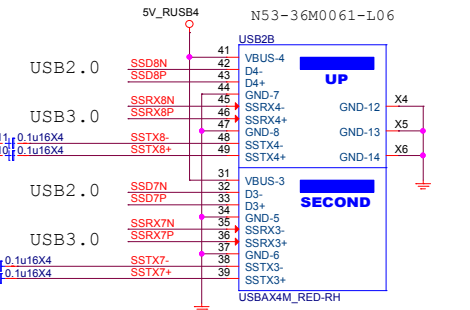
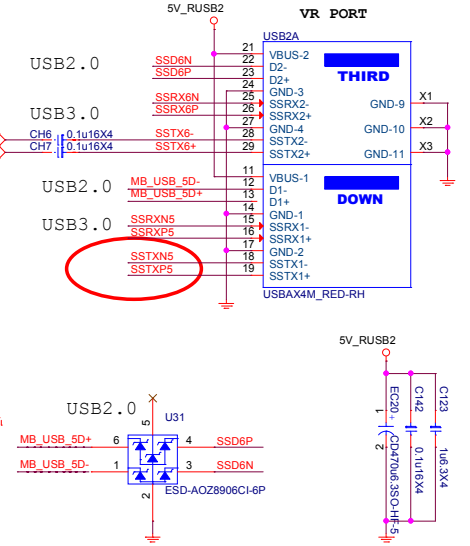


USB3.0

USB3.0



USB3.0



USB2.0

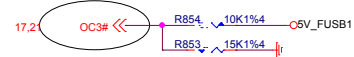
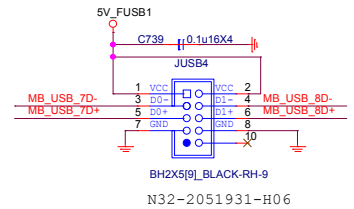
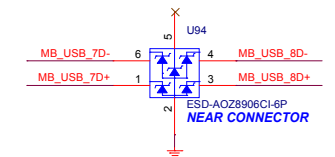
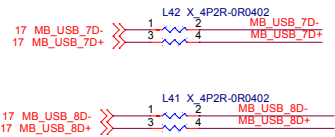


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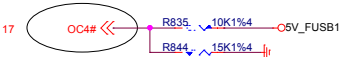
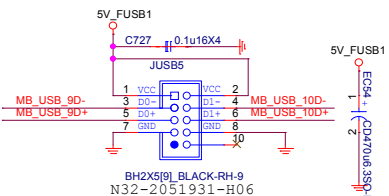
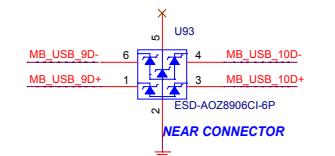
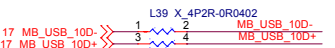
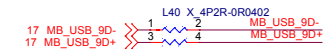
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Size	Document Description	Rev
Custom	REAR USB CONNECTOR	1.0
Date: Monday, May 15, 2017	Sheet 53 of 84	

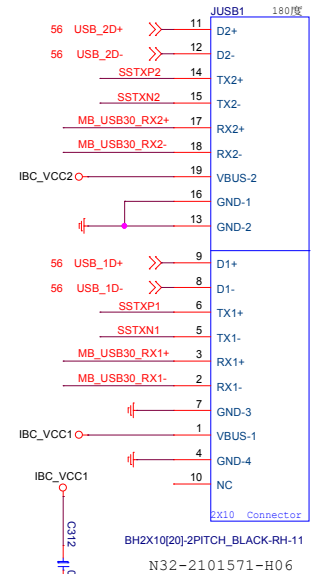
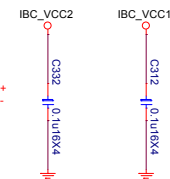
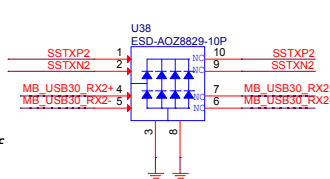
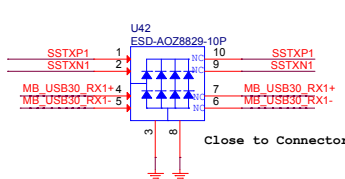
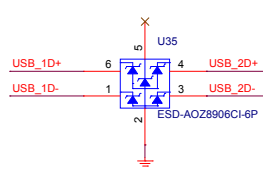
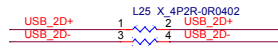
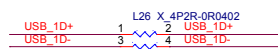
## FRONT USB PORT 7,8



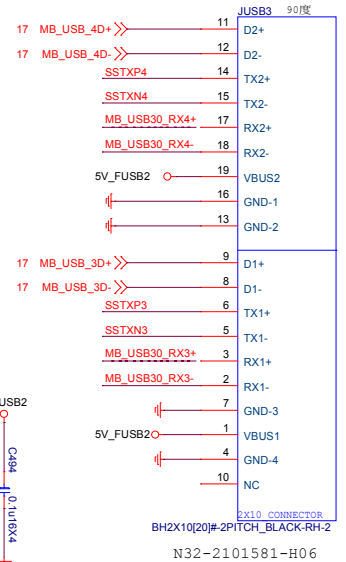
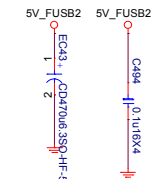
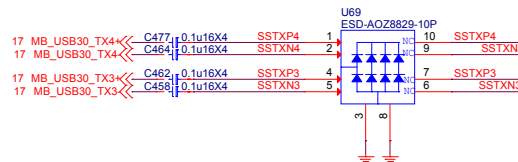
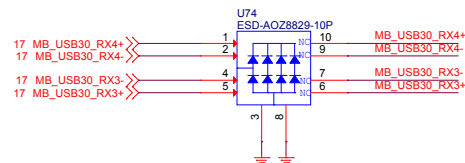
## FRONT USB PORT 9,10



0D先Remove Redriver



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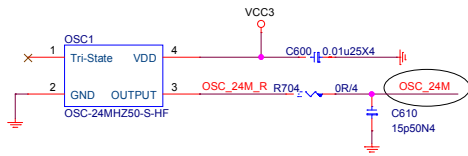
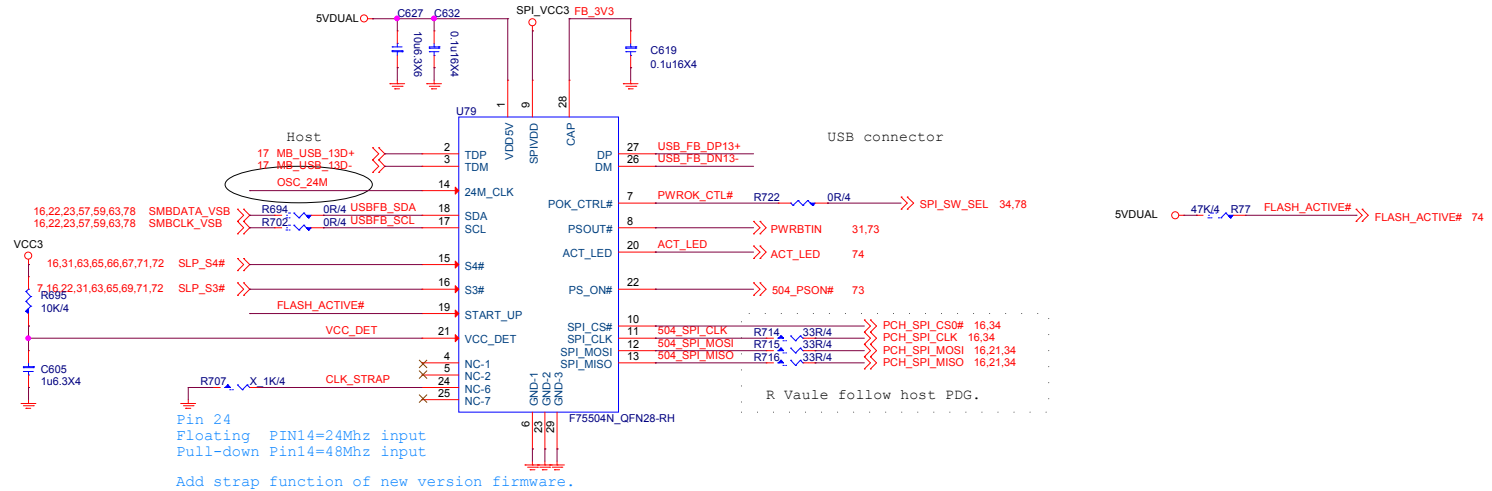
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Size	Document Description	Rev
Custom	Rear/Front USB2.0	1.0
Date: Monday, May 15, 2017	Sheet 54 of 84	

Host USB connector

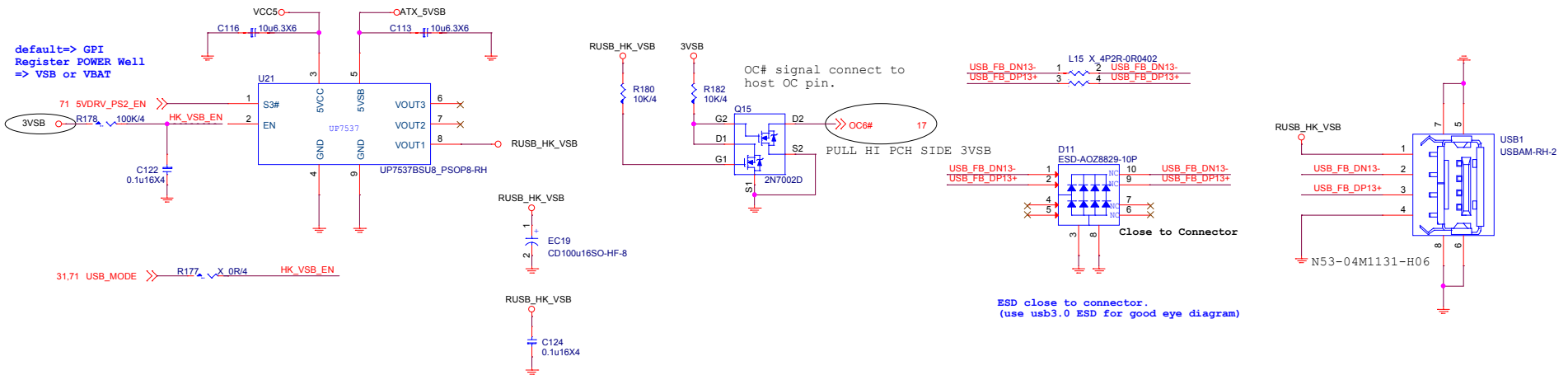
F75504 layout placement must meet to spi/usb trace length spec with host.  
As for as possible place near to host.



Reserved place to bottom, stub must be shortest.

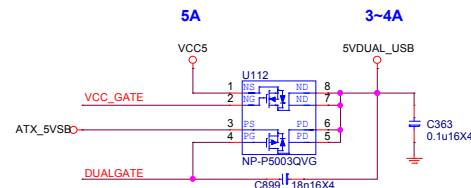
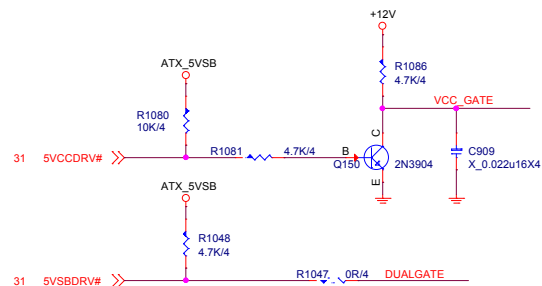
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USB Connector power come from UP7537 provide (USB Hotkey Connector same)

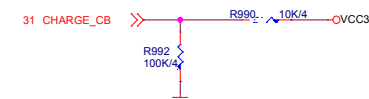




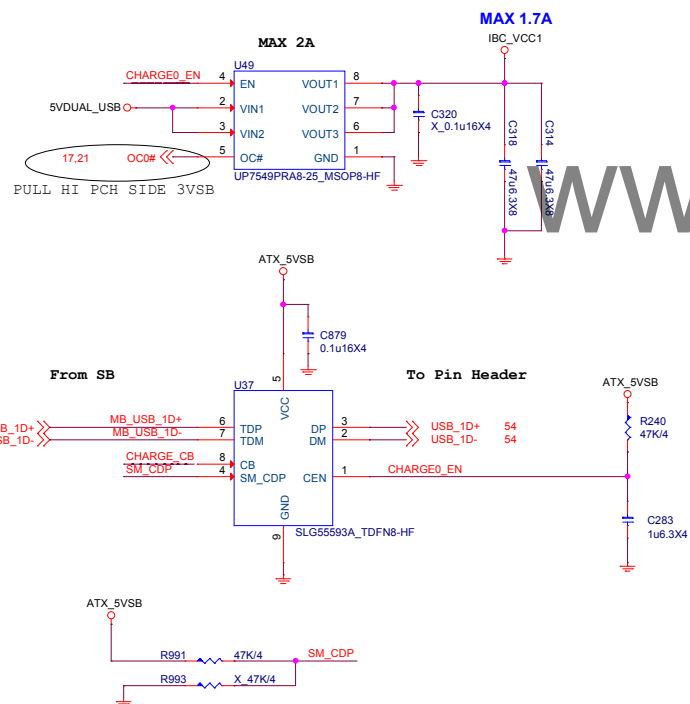
## 5VDUAL\_USB



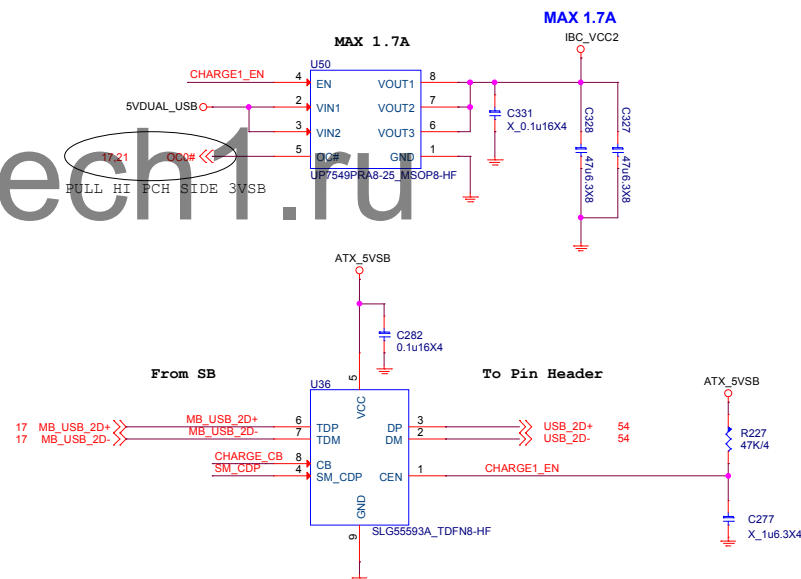
Pin power : I\_3VSB  
Register power : I\_3VSB  
Register reset : I\_3VSB



## USB POWER PORT 0 For USB Charging



## USB POWER PORT 1 For USB Charging

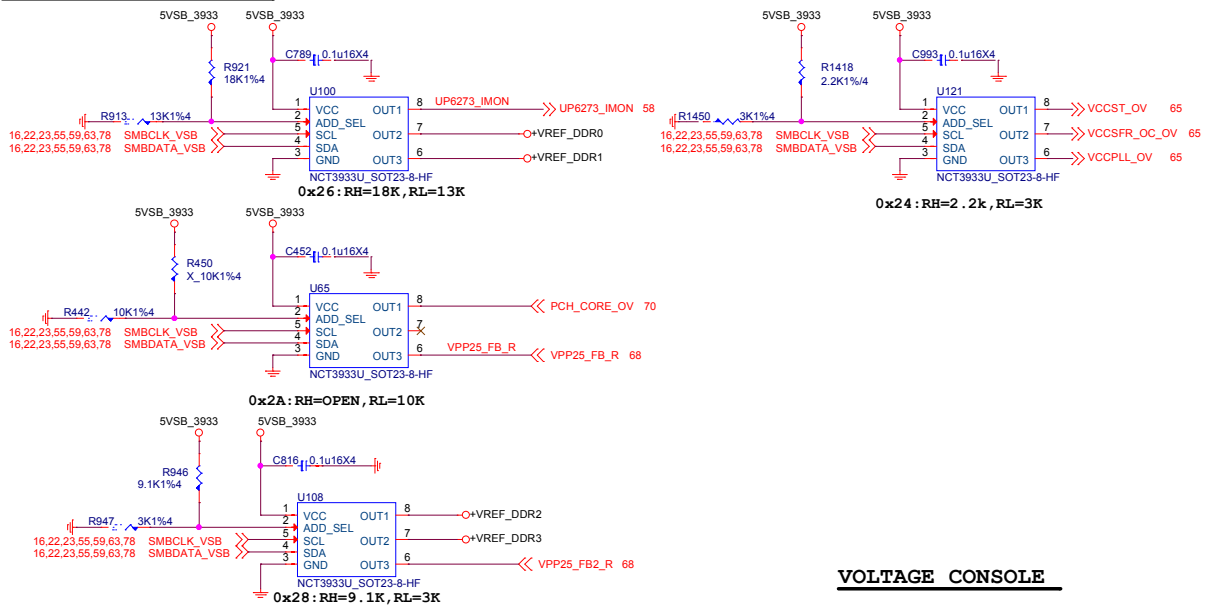


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Size	Document Description	Rev
Custom	USB CHARGE_SLG55593A	1.0
Date: Monday, May 15, 2017	Sheet 56 of 84	

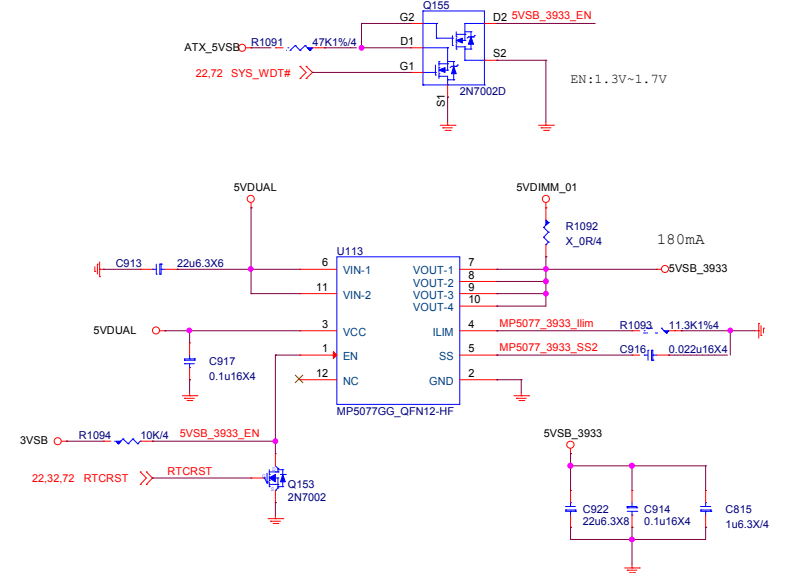
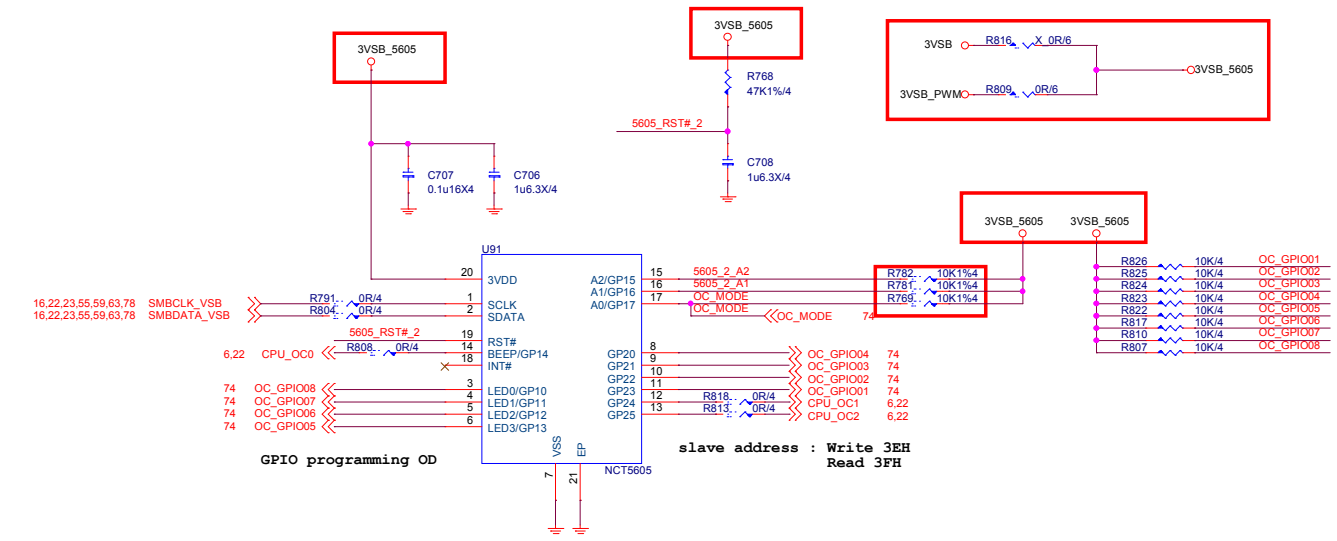
UPI VOLTAGE CONSOLE



VOLTAGE CONSOLE

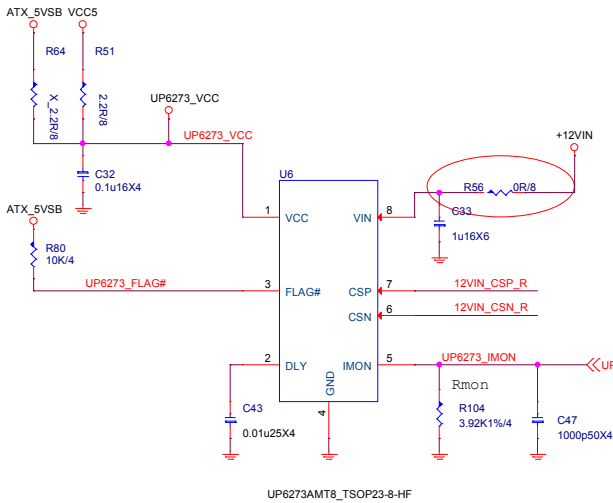
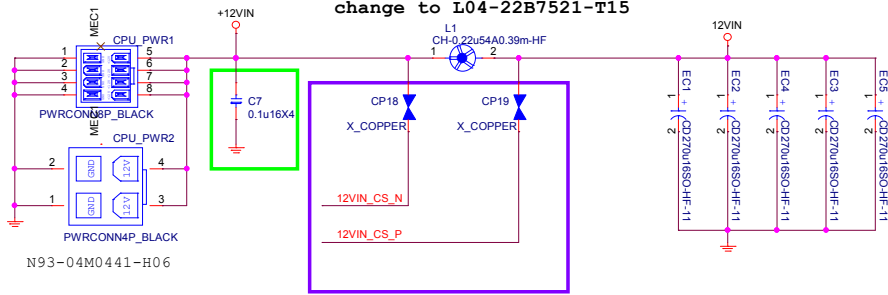
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.2	3	3.9	OPEN
BUS_SEL	0%	25%	42%	58%	75%	100%

RSVD FOR OC



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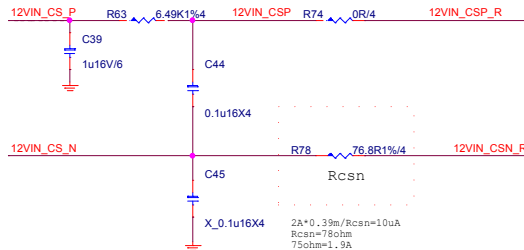
N93-08M0221-H06 Close Power Connector  
change to I04-22B7521-T15



$I_{in} = (V_{mon} \cdot R_{csn}) / (R_{mon} \cdot R_{dc})$   
 $V_{mon} = 1.2$   
can change OCP trigger level by Rcsn and Rmon

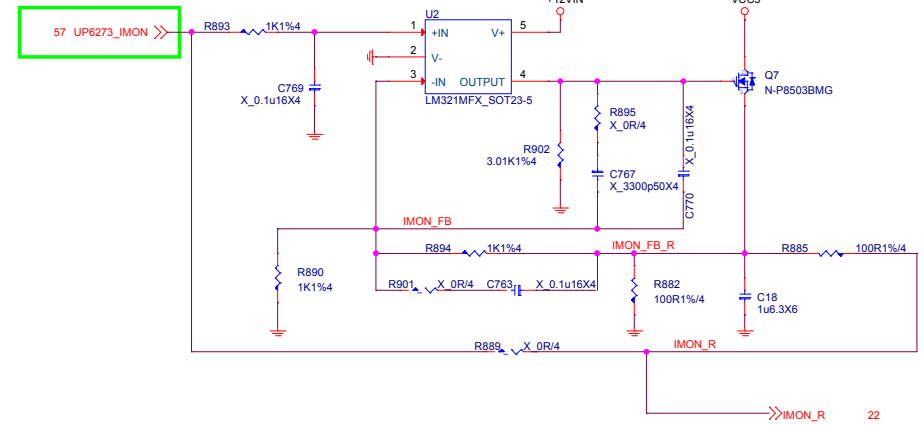
$R_{mon} = (1.2 \times 0.0768k) / (60 \times 0.39m)$   
 $= 3.9k$

—R80 2A  
Rmon5.1kOhm  
Rcsn0.0768kOhm  
DCR0.39mohm  
Vmon1.2V  
Iocp46.33484163A  
ocp=60A



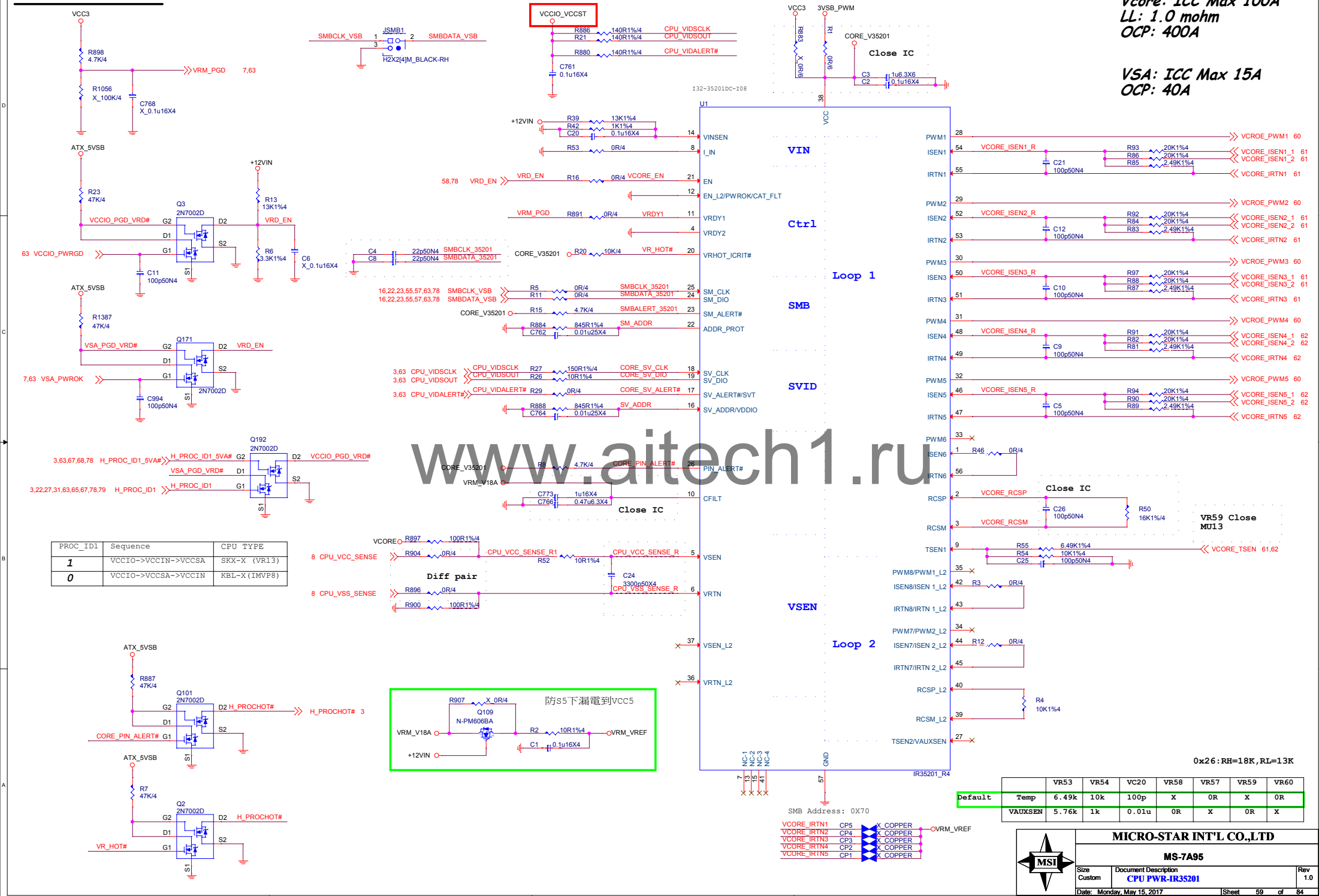
$2A \times 0.39m / R_{csn} = 10uA$   
 $R_{csn} = 78ohm$   
 $75ohm = 1.9A$

Near PWM IC

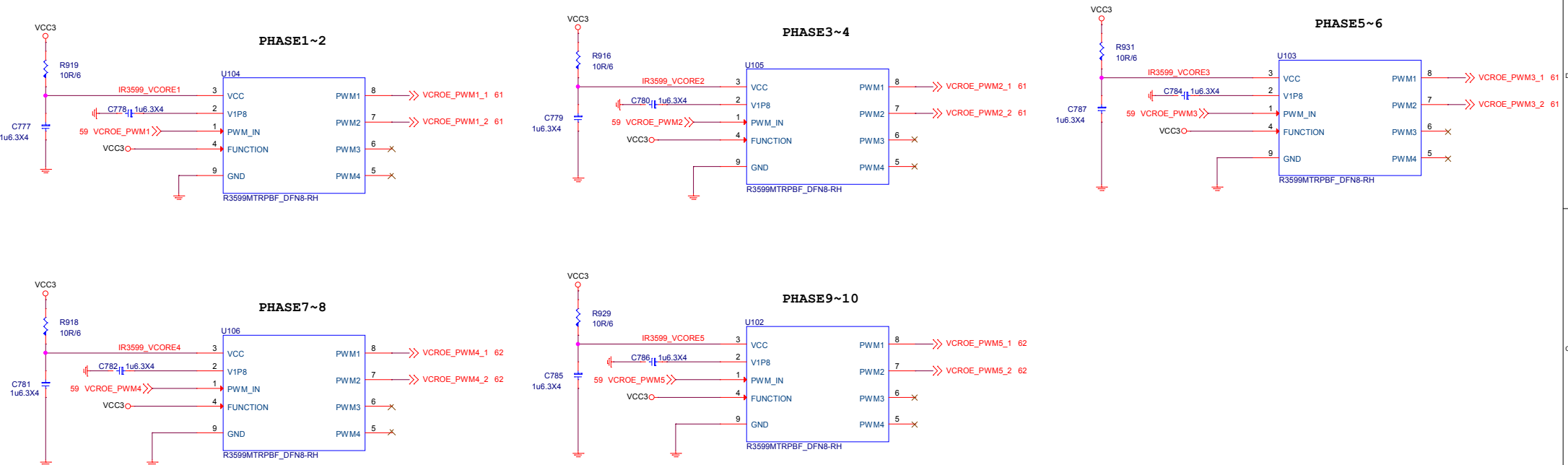


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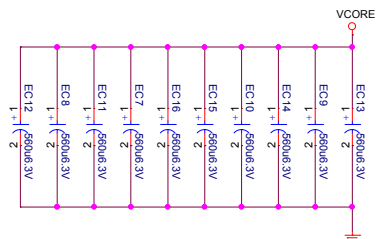
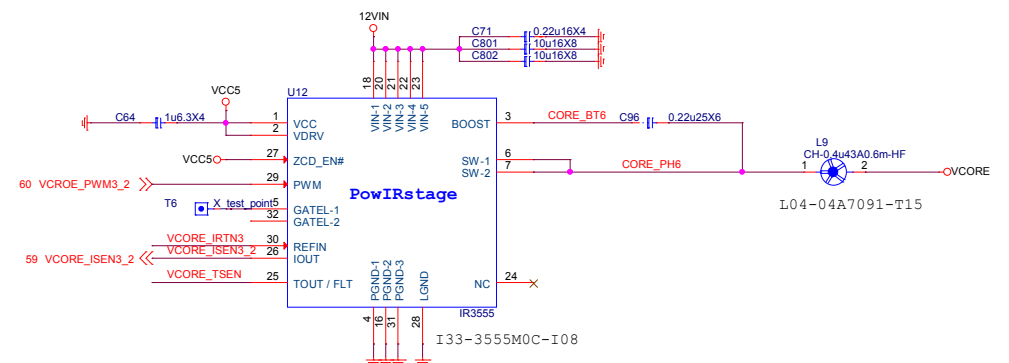
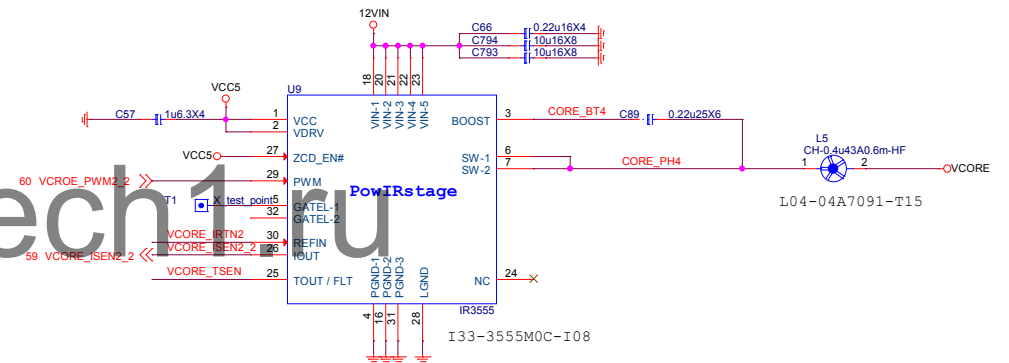
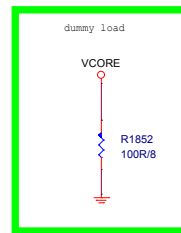
# VRMPWRGD LEVEL SHIFT



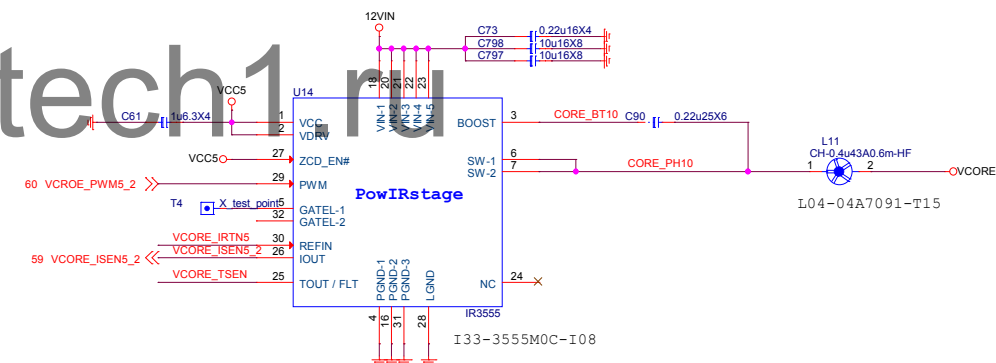
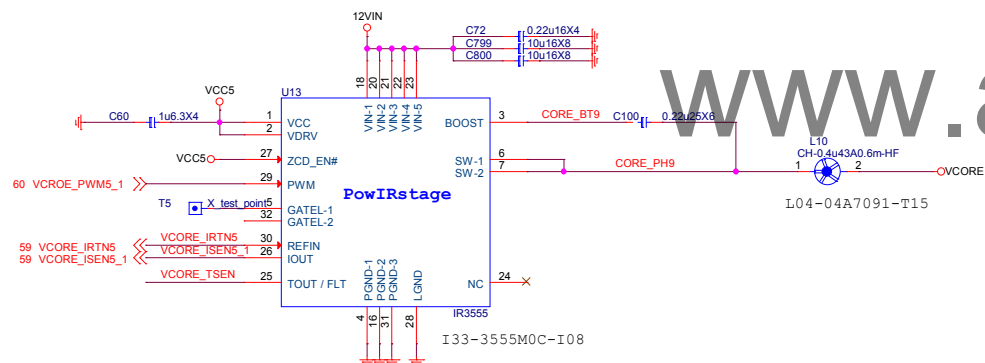
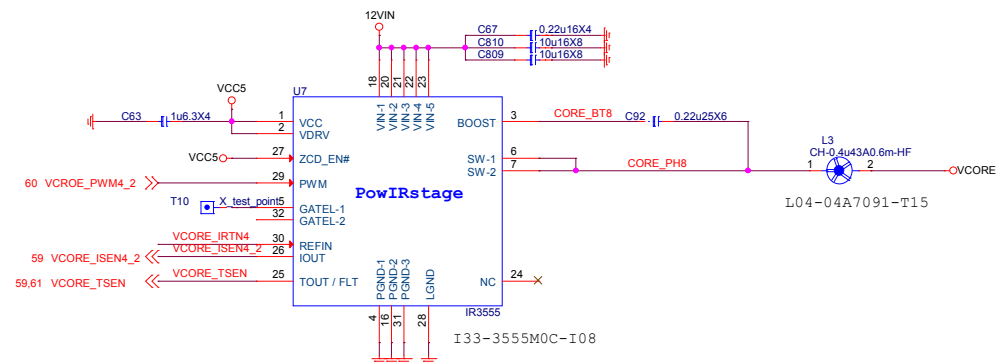
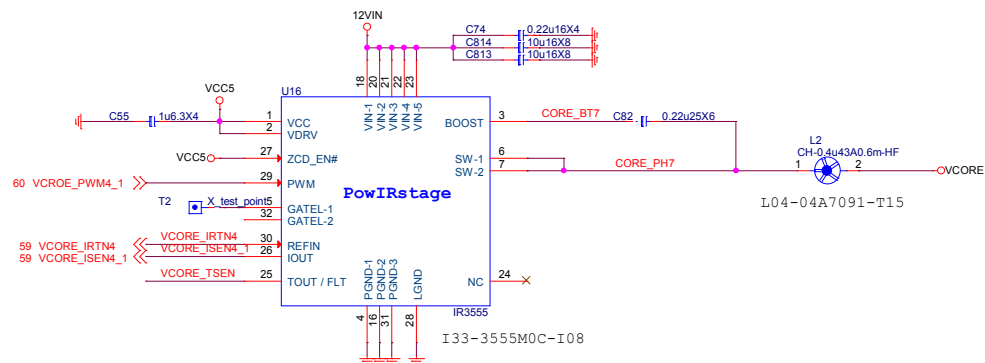
# VCORE Double



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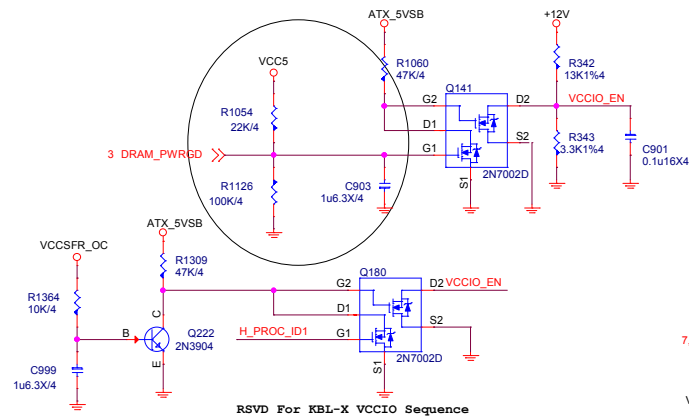
Size Custom	Document Description <b>CPU PWR-CORE-IR3555-PH1-6</b>	Rev 1.0
Date: Monday, May 15, 2017		Sheet 61 of 84



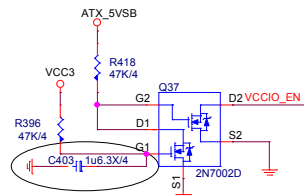
MICRO-STAR INT'L CO.,LTD		
MS-7A95		
Size	Document Description	Rev
Custom	CPU PWR-CORE-IR3555-PH7-10	1.0
Date: Monday, May 15, 2017		Sheet 62 of 84



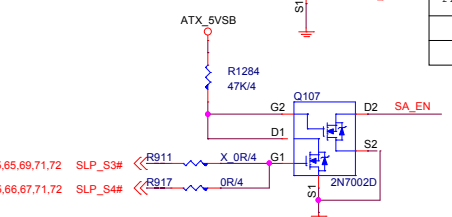
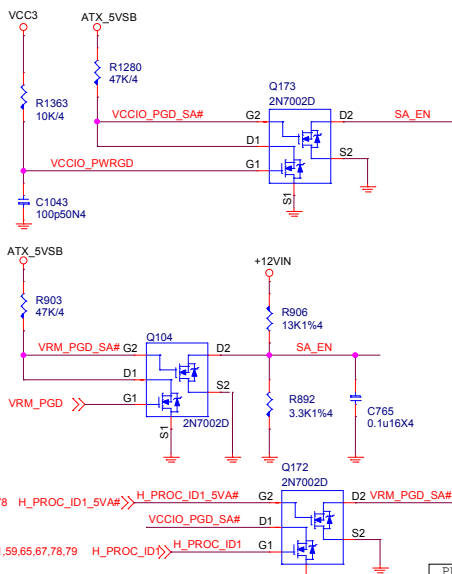
## VCCIOPWRGD LEVEL SHIFT



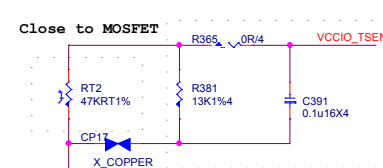
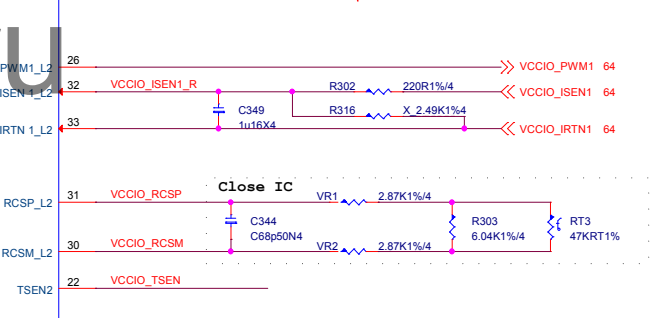
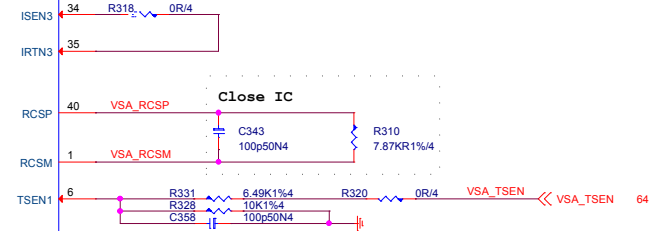
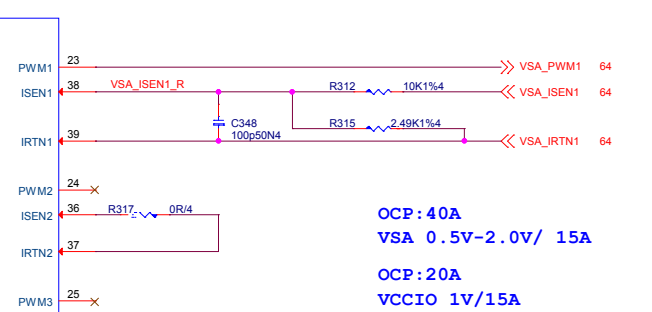
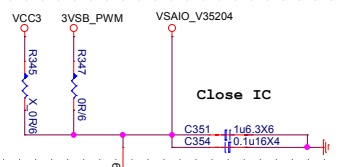
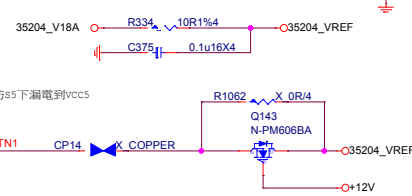
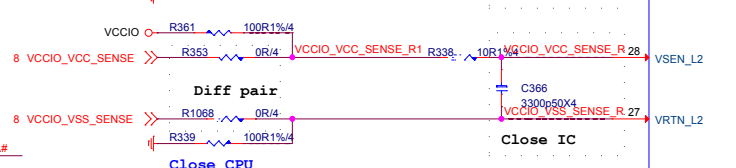
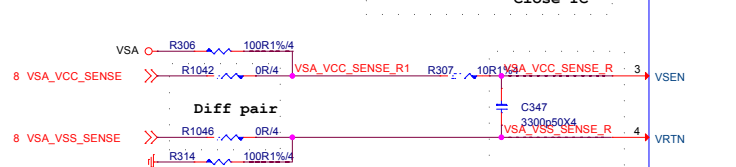
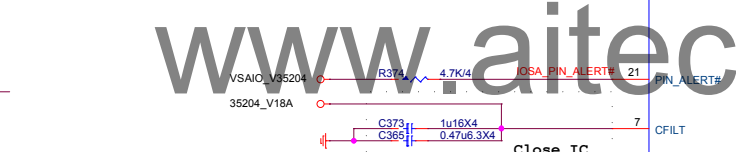
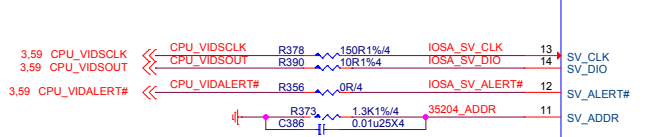
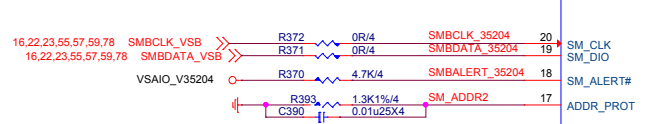
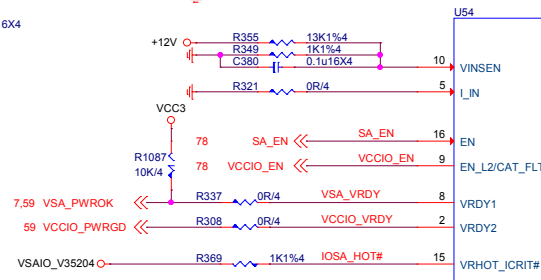
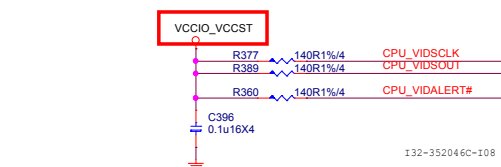
### RSVD For KBL-X VCCIO Sequence



確保S3回來，VCCIO比VCC3晚起來。不會造成停00 20170124



PROC_ID1	Sequence	CPU TYPE
<b>1</b>	VCCIO->VCCIN->VCCSA	SKX-X (VRI3)
<b>0</b>	VCCIO->VCCSA->VCCIN	KBL-X (IMVP8)



CPU ID CFG		
PROC_ID1	PROC_ID0	CPU TYPE
0	0	future CPU(IMVP9)
0	1	KBL-X(IMVP8)
1	0	future CPU
1	1	SKX-X (VR13)

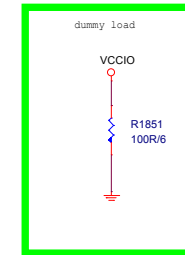
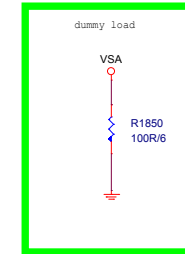
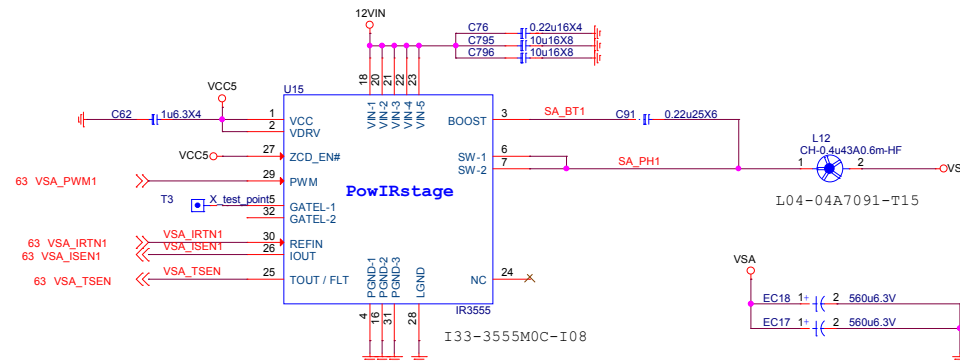


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**MS-7A95**

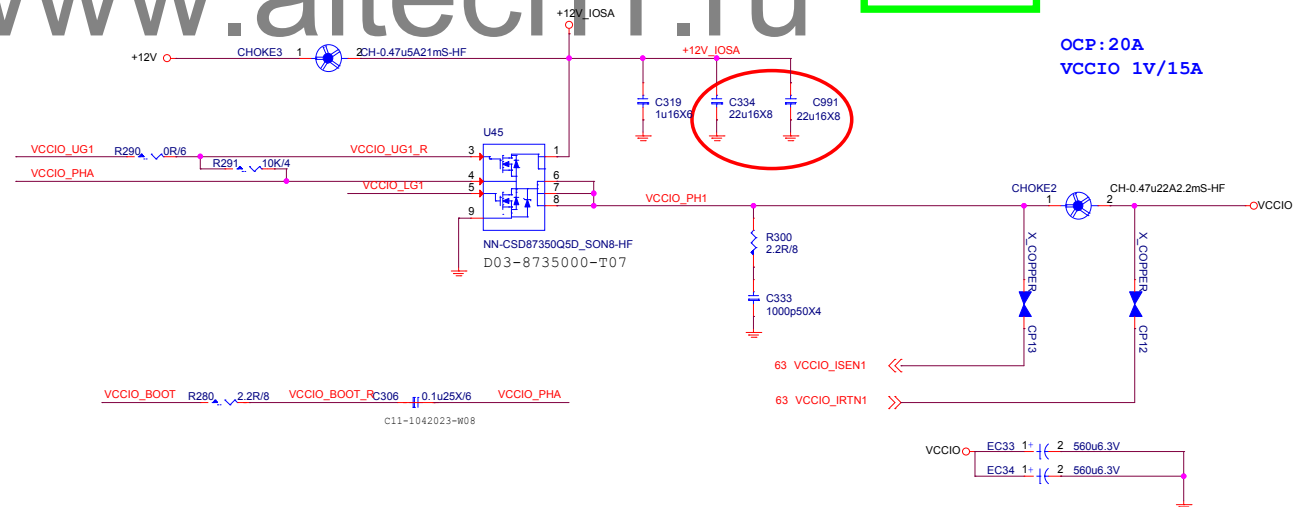
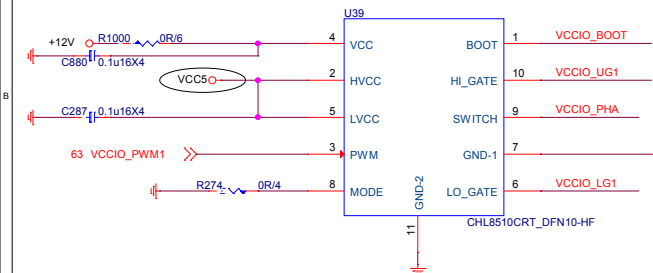
Size Custom	Document Description <b>VR13_VSA/VCCIO IR35204</b>	Rev 1.0
Date: Monday, May 15, 2017		Sheet 63 of 84

OCP:40A  
VSA 0.5V-2.0V/ 15A



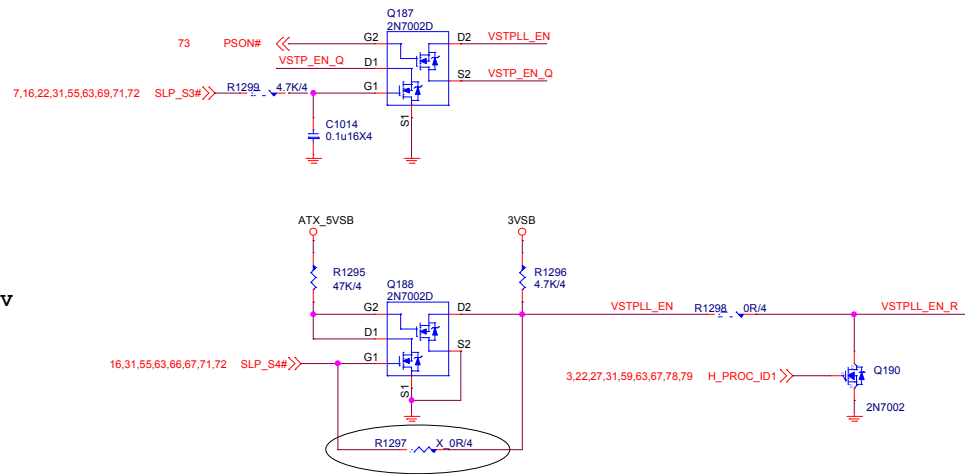
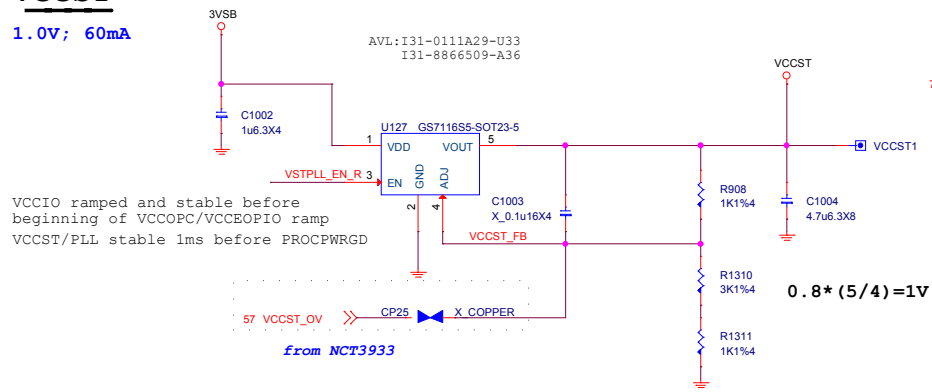
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OCP:20A  
VCCIO 1V/15A



## VCCST

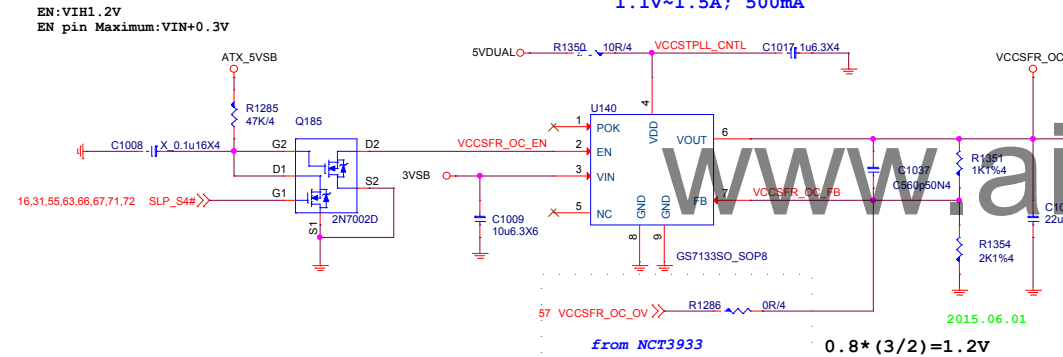
1.0V; 60mA



For non-OC system, configures +VCCSFR\_OC as 1.2V

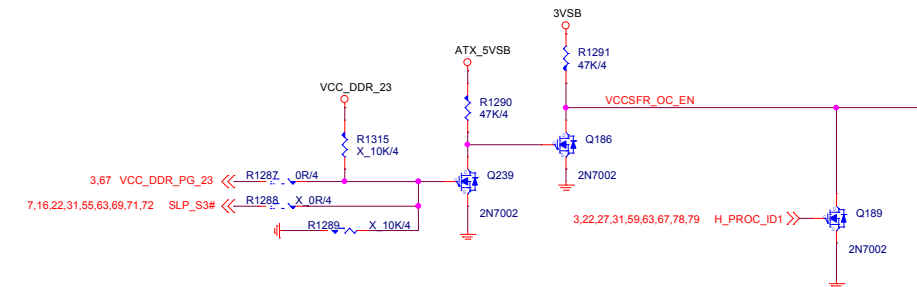
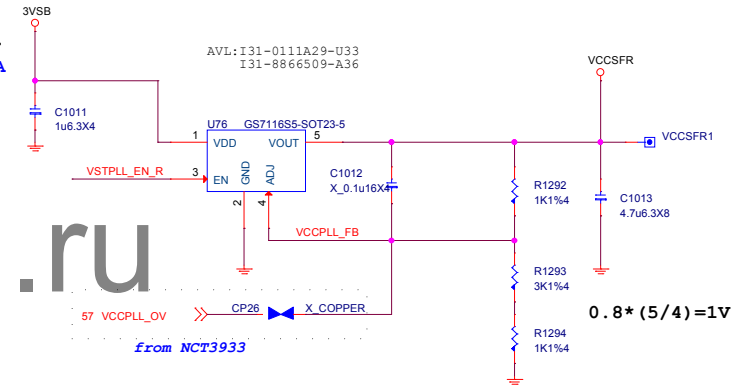
## VCCSFR\_OC

1.1V~1.5A; 500mA



## VCCSFR

1.0V; 150mA



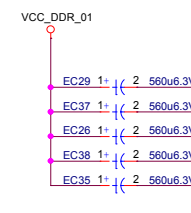
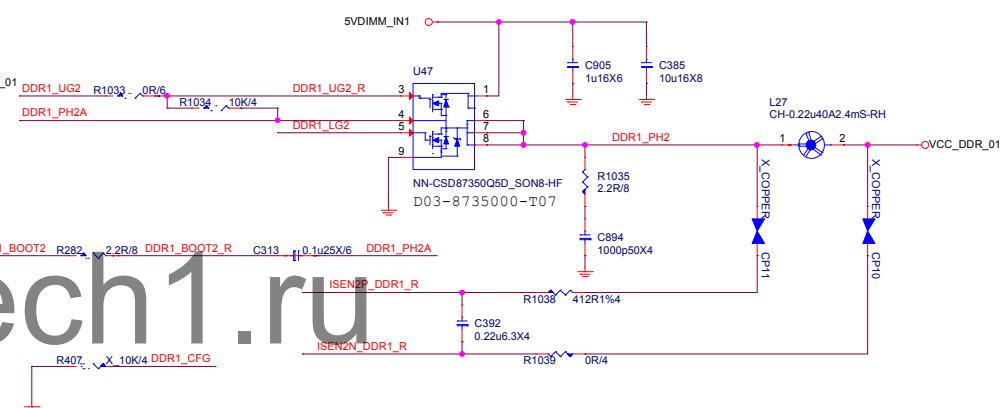
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MS-7A90

Size Custom Document Description CPU VCCST/VCCSFR/VCCSFR\_OC Rev 10

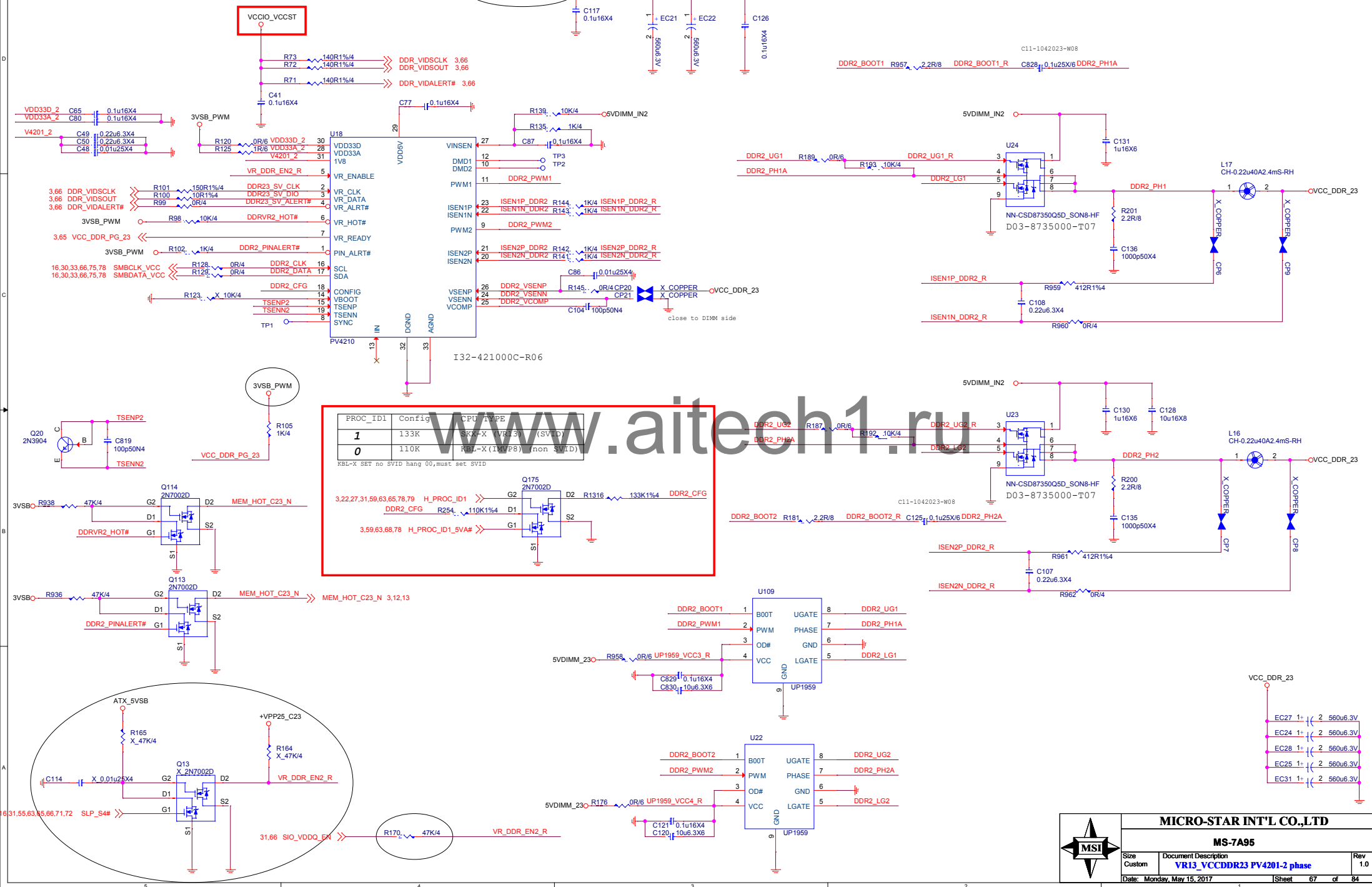
Date: Monday, May 15, 2017 Sheet 65 of 84

**DDR4 1.2V nominal,  
0.8V-2.5V Max, 44.14A / OCP 50A**



Size Custom	Document Description <b>VR13_VCCDDR01 PV4201-2 phase</b>	Rev 1.0
Date: Monday, May 15, 2017	Sheet 66 of 84	

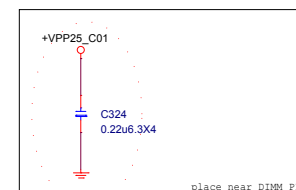
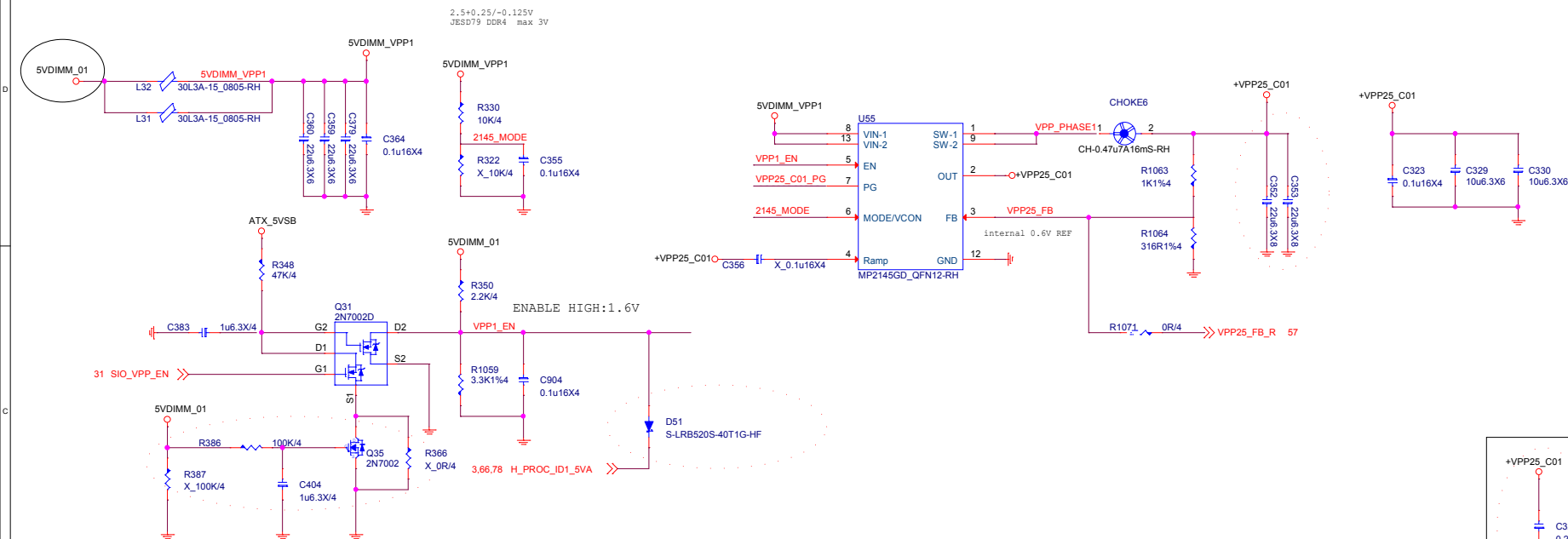
DDR4 1.2V nominal,  
0.8V-2.5V Max, 44.14A / OCP 50A



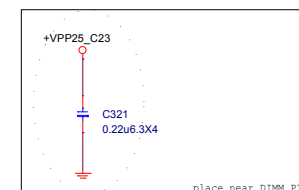
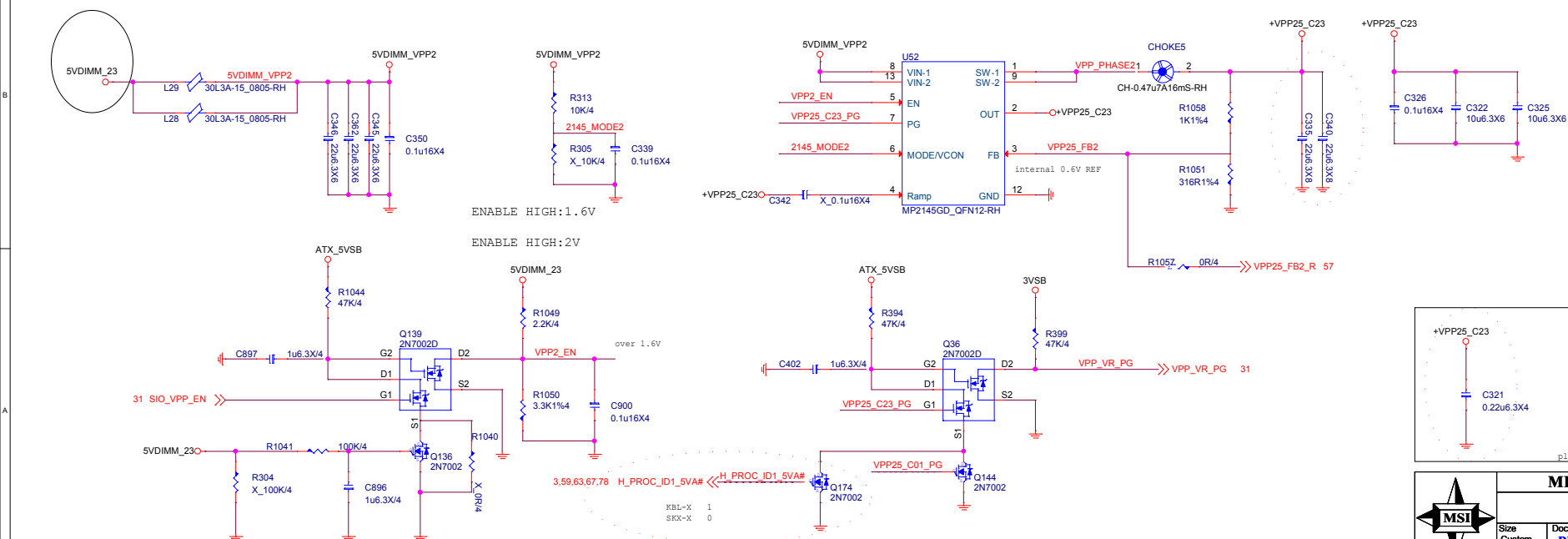
MS-7A95

Size Custom	Document Description <b>VR13_VCCDDR23 PV4201-2 phase</b>	Rev 1.0
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4DIMM :6A FOR DDR VPP



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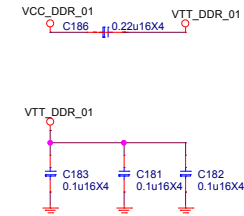
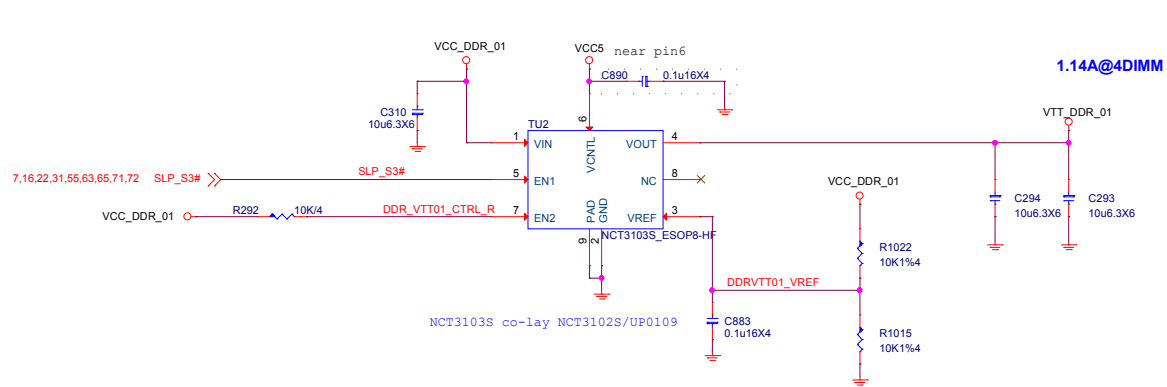
Size	Document Description
Custom	<b>DDR Power-VPP25</b>

Rev	1.0
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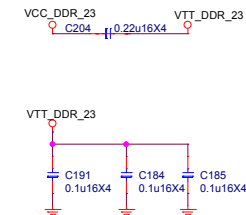
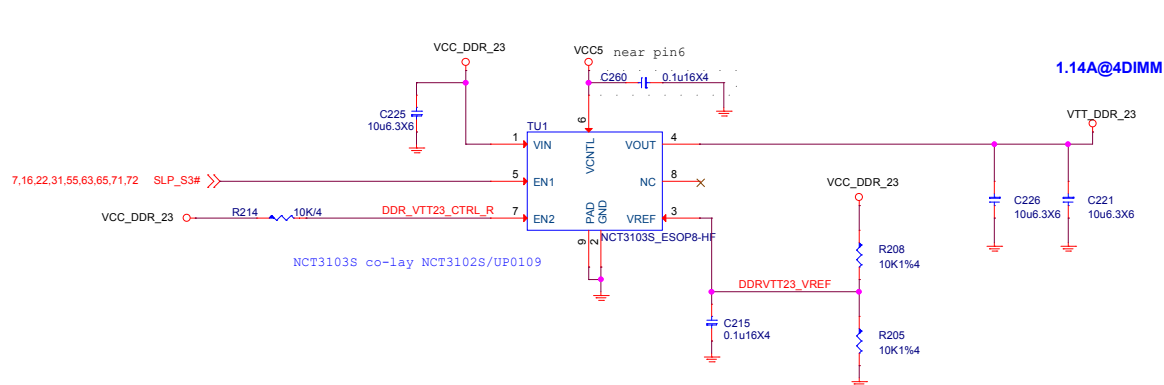
### DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



### DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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# PCH\_1VSB Power:1.0V,10A

$$\begin{aligned} I_{rms} &= I_{out} * \sqrt{((V_{out}/V_{in}) * (1 - (V_{out}/V_{in})))} \\ &= 10.664 * 0.4 \\ &= 4.2656A < 5000mA \end{aligned}$$

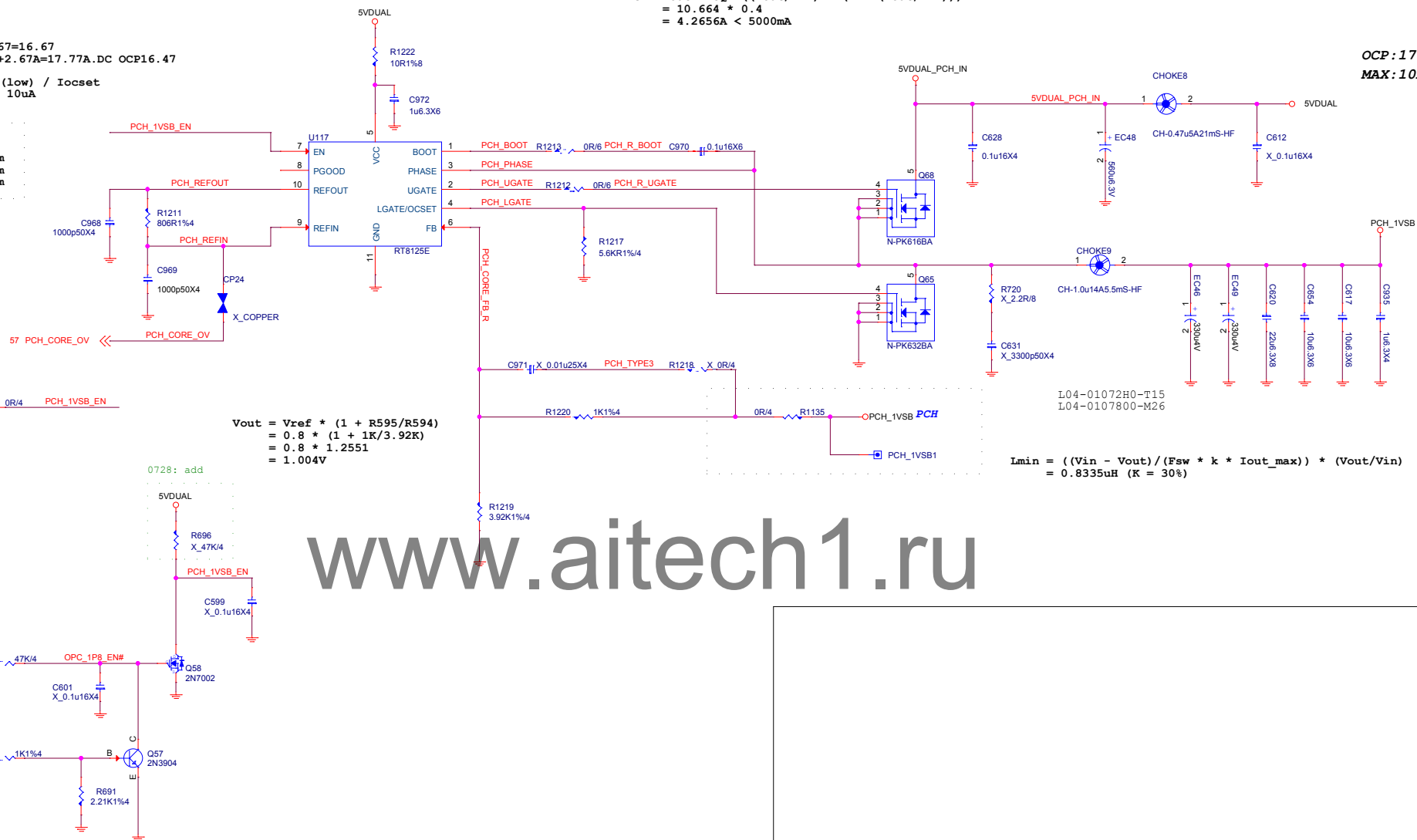
OCF:17.77  
MAX:10A

OCF = 14A R597=5.6K  
IOCP=10uA\*5.6K/0.004=14A +2.67=16.67  
\*IOCP=10uA\*6.04/0.004 =15.1A+2.67A=17.77A.DC OCF16.47

Rocset = 1.5 \* I<sub>max</sub> \* R<sub>dson(LOW)</sub> / Iocset  
= 1.5 \* 10 \* 4mohm / 10uA  
= 6K

## Rdson (low)

D03-4C05N03-O05 : 3.4mohm  
D03-632BA0C-N03 : 3.3mohm  
D03-3056M00-U47 : 4.2mohm



$$\begin{aligned} L_{min} &= ((V_{in} - V_{out}) / (F_{sw} * k * I_{out\_max})) * (V_{out}/V_{in}) \\ &= 0.8335uH (K = 30\%) \end{aligned}$$

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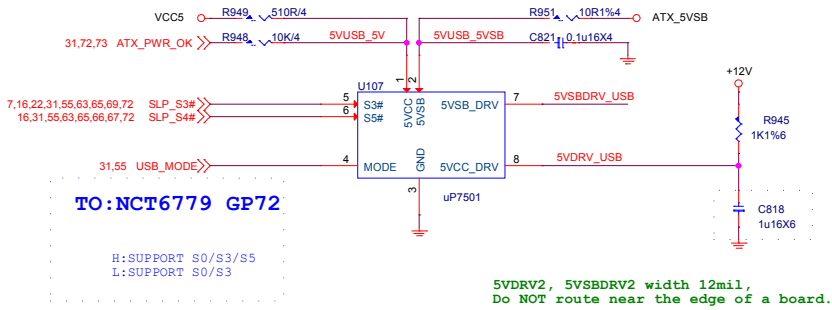


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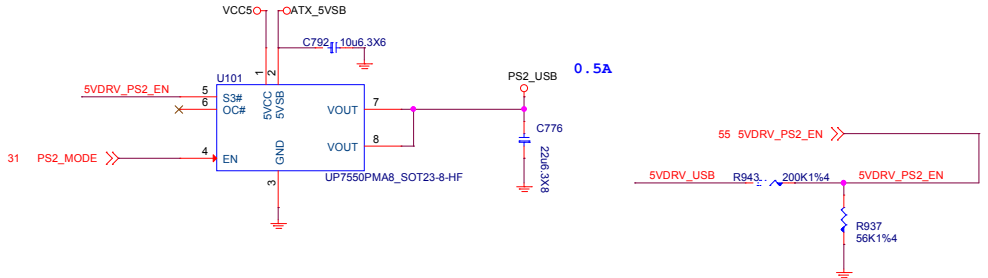
MS-7A95

Size	Document Description	Rev
Custom	PCH POWER-RT8125E	1.0
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USB POWER

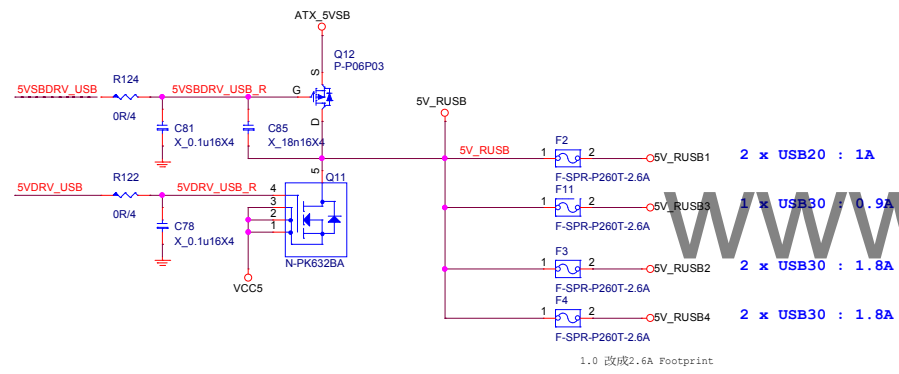


PS2 POWER

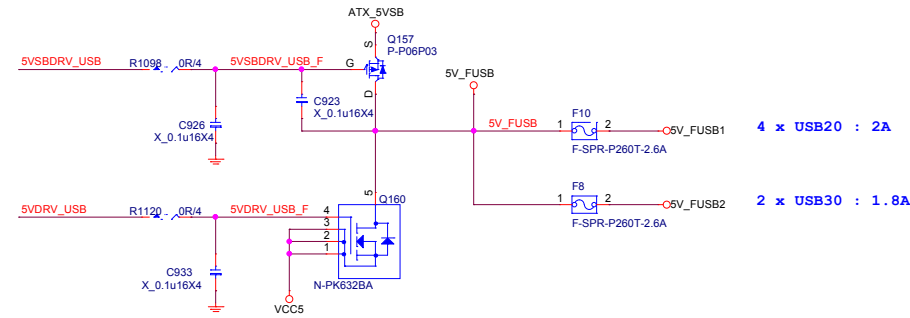


USB MODE

REAR USB PORT POWER



FRONT USB PORT POWER



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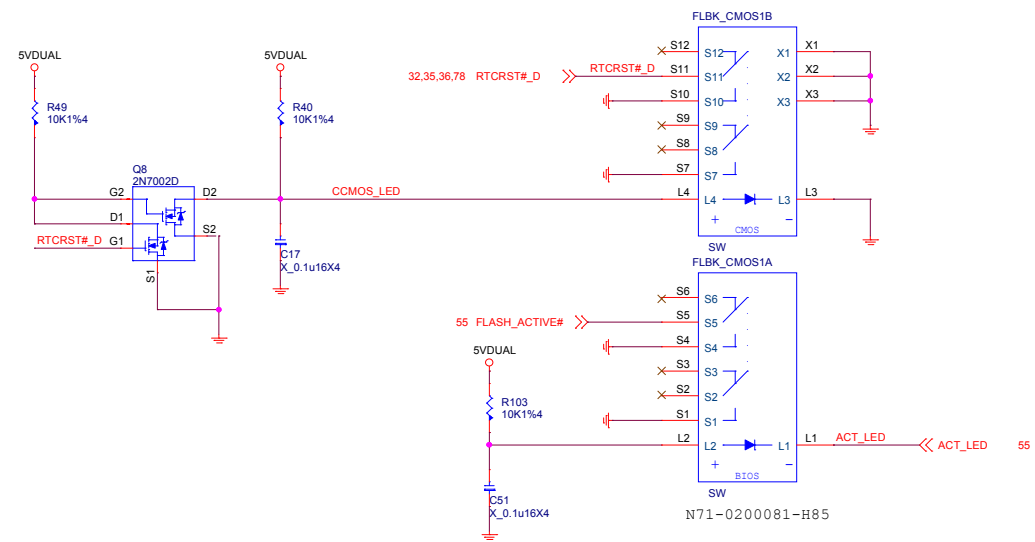
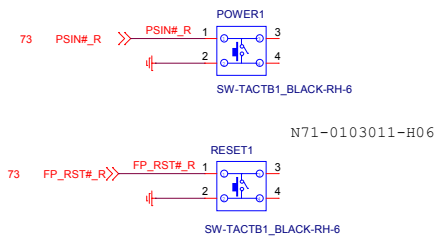
**MS-7A95**

Size Custom	Document Description <b>USB Power</b>	Rev 1.0
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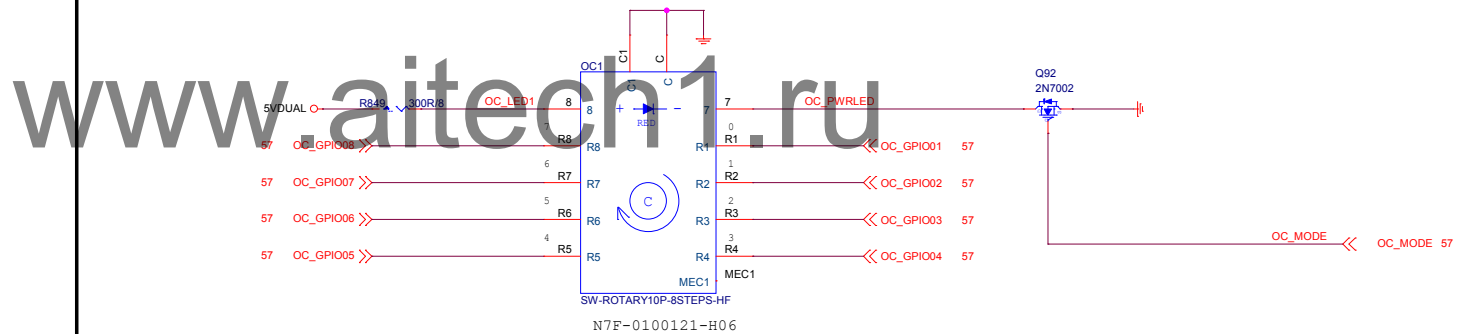




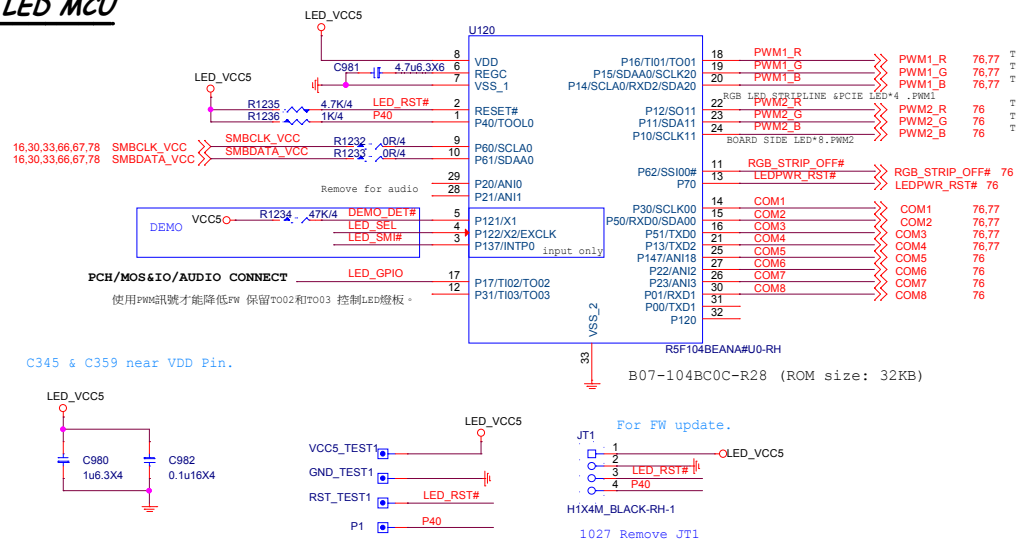
PWR/RST Botton



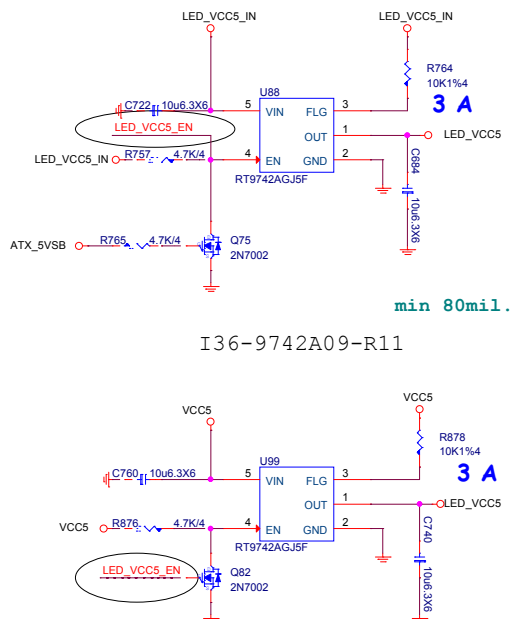
OC Genie



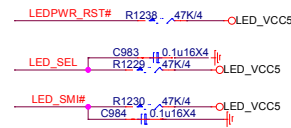
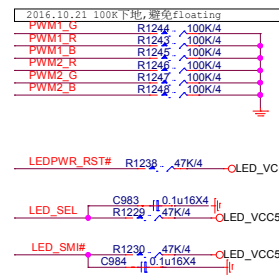
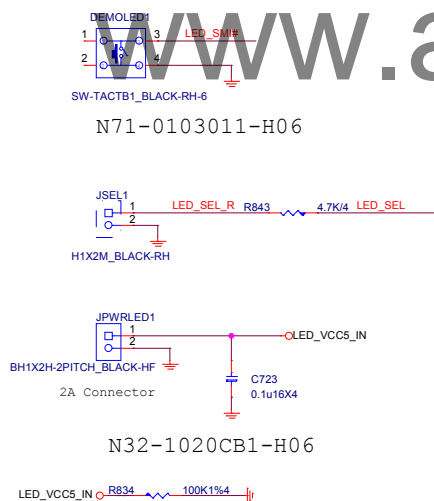
## LED MCU



### EXTERNAL POWER INPUT

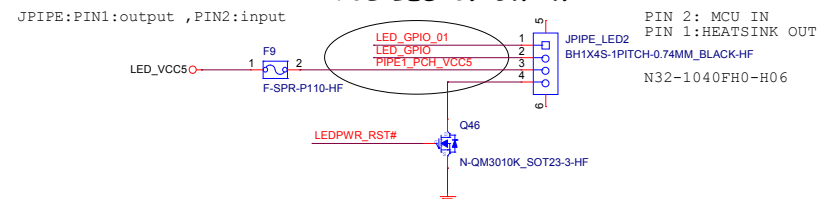


## LED Demo Button



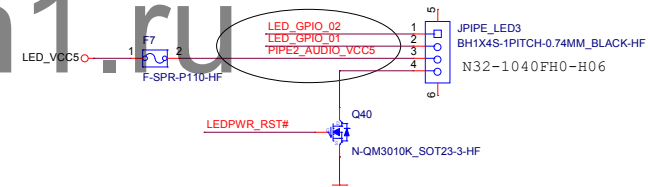
1 PCH HEATSINK LED

**PCS LED\*0.16W=W**



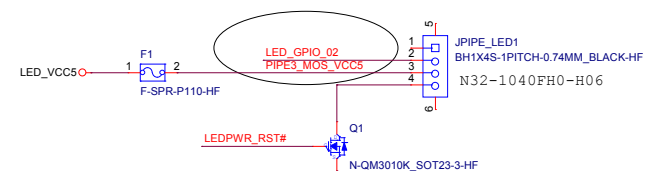
## 2 AUDIO/IO Cover LED

**PCS LED\*0.16W=W**



**MOS HEATSINK LED**

**PCS LED\*0.16W=W**



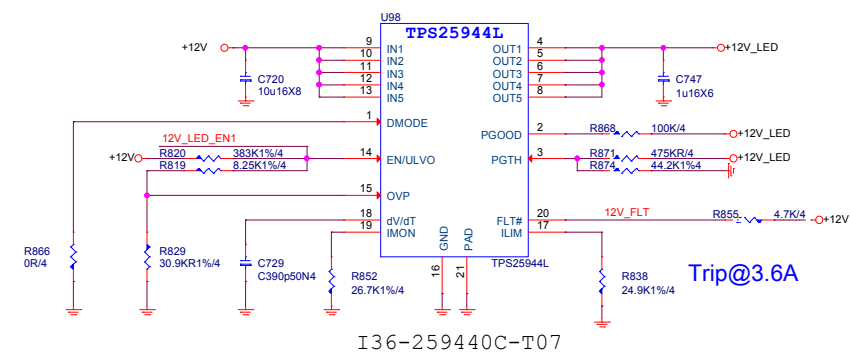
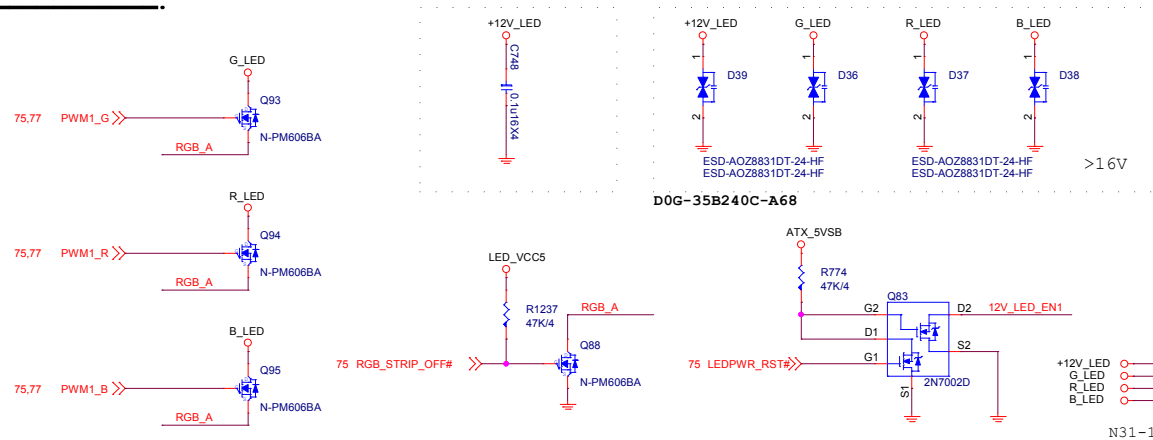
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**MS-7A95**

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# LED STRIPLINE

2016.07.06 only reserve now  
2016.08.02 Add +12V\_LED 0.1uF  
2016.08.02 stuff ESD



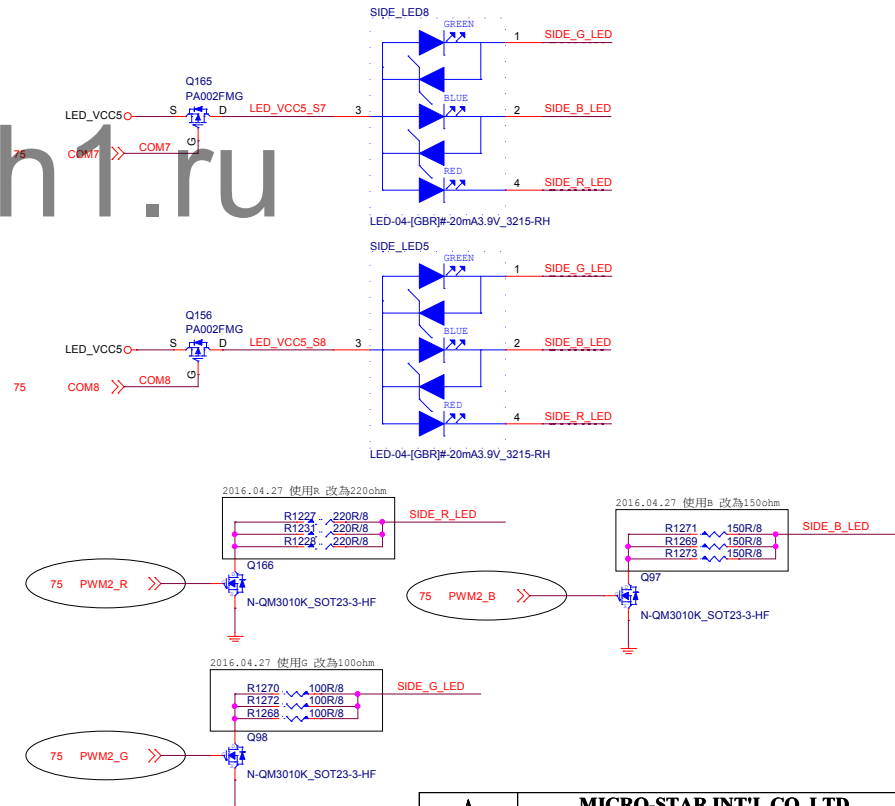
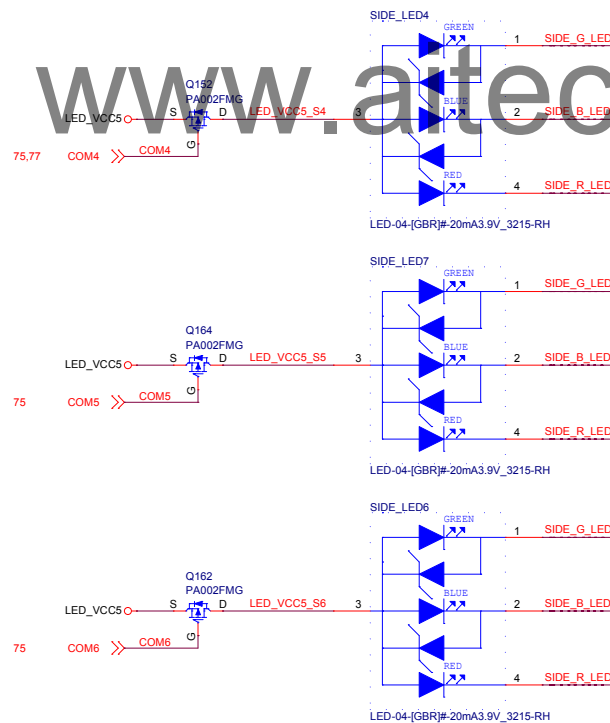
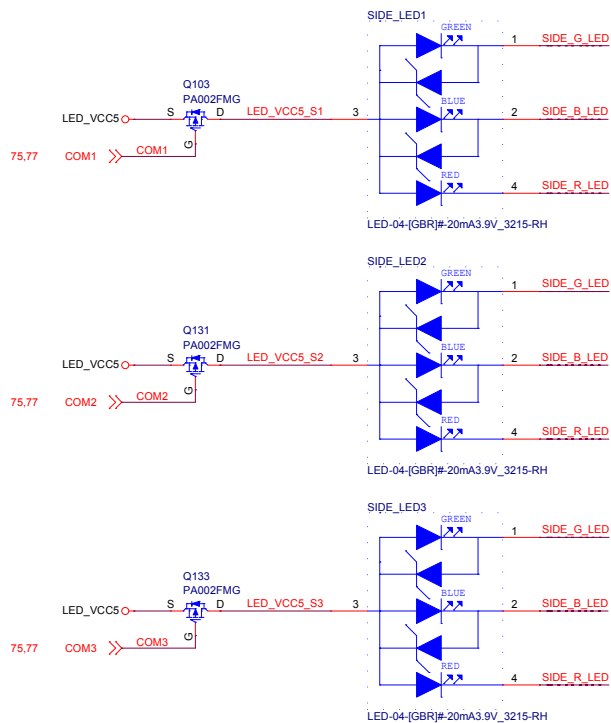
外接LED 燈條 (RGB )

---- PCB 文字面 (JLED1)

---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺 (待7A20驗證)

## BOARD SIDE LED \*8

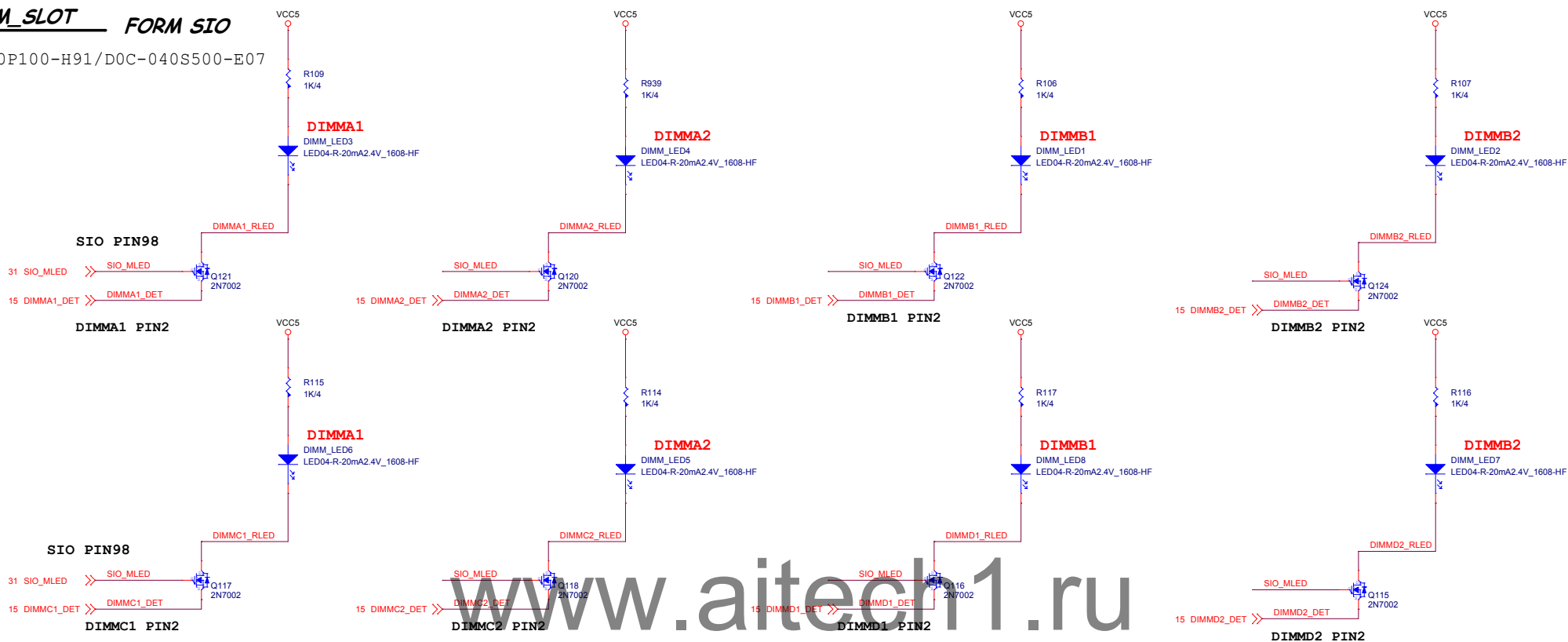
D0C-040R700-H91  
Forward Current 20mA  
Pulse Forward Current 30-60mA





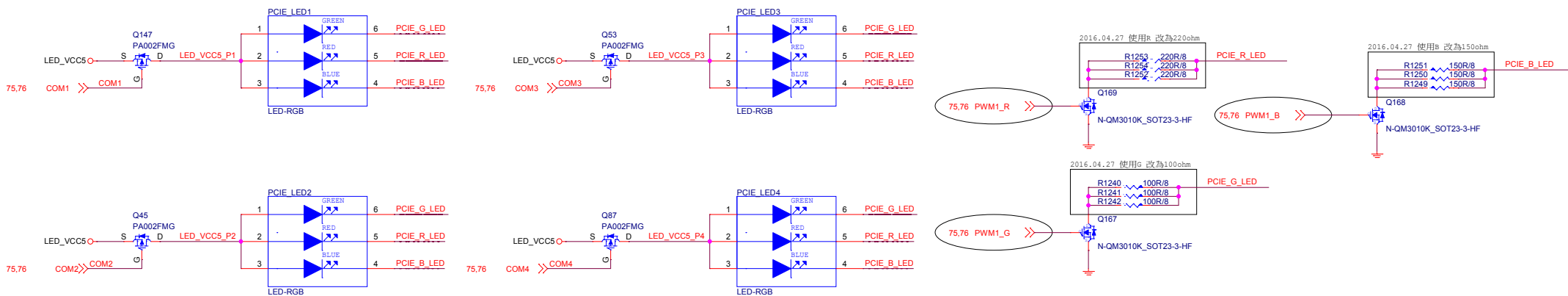
# DIMM\_SLOT FORM SIO

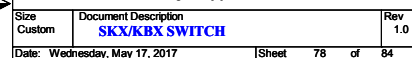
D0C-040P100-H91/D0C-040S500-E07



# PCIE\_SLOT LED\*4 FORM MCU

D0C-040S400-H91

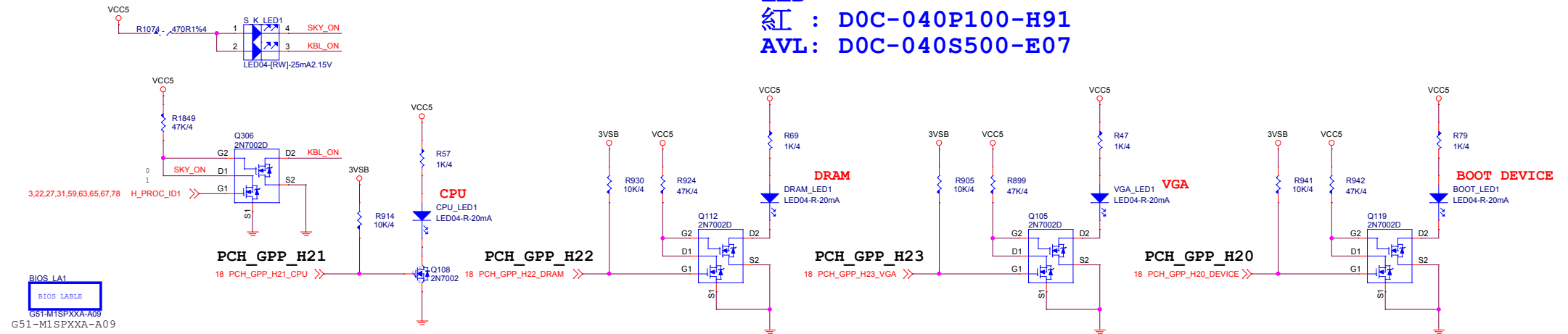




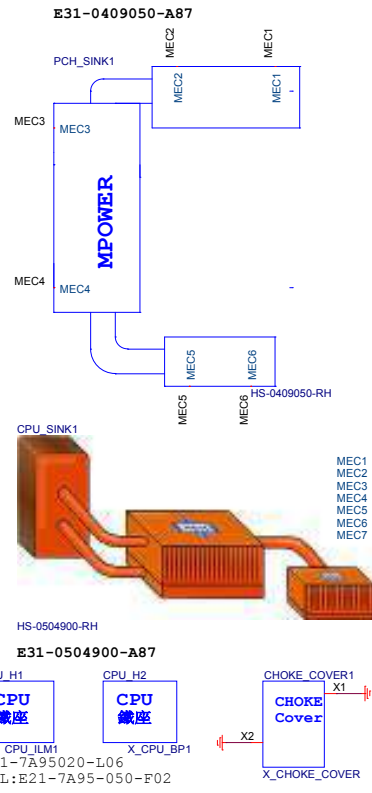
# LED

## 紅 : DOC-040P100-H91

## AVL: DOC-040S500-E07



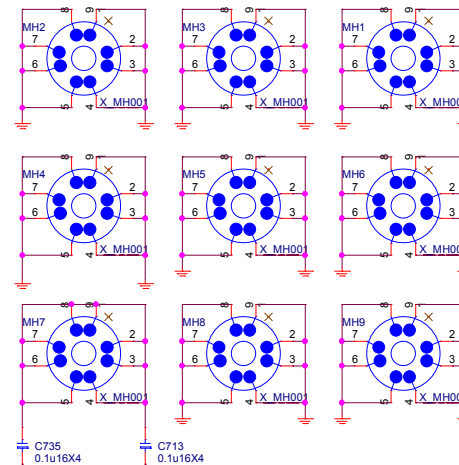
BIOS LA1  
G51-M1SPXXA-A09  
SLH1  
Label  
VIRTUAL  
Y01-RNVIDIL-000  
SSE1  
Label  
VIRTUAL  
Y02-MA00101-SSE  
XSPLT1  
Label  
VIRTUAL  
Y02-MA00401-XSP  
NAHIMIC1  
Label  
VIRTUAL  
Y02-MU00100-NAH  
CFOS1  
Label  
VIRTUAL  
Y02-MU00170-CFO  
MKT1  
Label  
VIRTUAL  
G51-M1SPL72-Q13



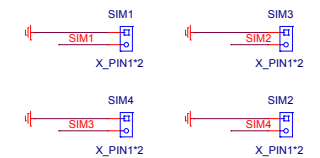
GPIO LED	GPP_H21	GPP_H22	GPP_H23	GPP_H20
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

- 開機斷電狀態下，4個LED先維持default全暗，開機通電後：
1. 首先進行CPU check CPU LED 亮，check PASS後則CPU LED減掉。
  2. 接著依序進行Memory /memory LED亮check PASS後則memory LED減掉。
  3. VGA的check/VGA LED亮，check PASS後則VGA LED減掉。
  4. BOOT DEVICE的check/BOOT LED亮，check PASS後則BOOT LED減掉。
  5. 因此最後正常順利開機後，四個LED燈都是減掉的。  
(系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作)

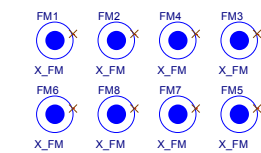
### Mounting Holes



### Simulation



### Optical Fiducial Marks-120



VCCORE VCCIN1  
VSA VCCSA1  
VCCIO VCCIO1  
VCC\_DDR\_01 VCC\_DDR\_01  
VCC\_DDR\_23 VCC\_DDR\_23  
VTT\_DDR\_23 VTT\_DDR\_23  
VTT\_DDR\_01 VTT\_DDR\_01  
5VDUAL 5VDUAL1  
5VDIMM\_01 5VDIMM\_01  
5VDIMM\_23 5VDIMM\_23  
3VSB 3VSB1  
VBAT VBAT1  
+VPP25\_C23 VPP25\_C23  
+VPP25\_C01 VPP25\_C01